YASKAWA

VIPA System 300S

CP | 342-2IA71 | Manual

HB140 | CP | 342-2IA71 | en | 17-22

SPEED7 CP 342S-2IBS

www.vipa.com/en/service-support/manual

VIPA CONTROLS

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342-2IA71_000_CP 342S-2IBS,1,EN - © 2017

Table of contents

1 General

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1.2 About this manual

Objective and contents

This manual describes the CP 342-2IA71 of the System 300S from VIPA. It contains a description of the construction, project implementation and usage.

Product	Order number	as of state:	
		CP-HW	CP-FW
CP 342S-2IBS	342-2IA71	01	V1.0.0

Target audience

The manual is targeted at users who have a background in automation technology.

Structure of the manual

The manual consists of chapters. Every chapter provides a self-contained description of a specific topic.

Guide to the document

The following guides are available in the manual:

- An overall table of contents at the beginning of the manual
- References with page numbers

Availability

The manual is available in:

- printed form, on paper
- in electronic form as PDF-file (Adobe Acrobat Reader)

Icons Headings

Important passages in the text are highlighted by following icons and headings:

DANGER!
Immediate or likely danger. Personal injury is possible.

CAUTION!
Damages to property is likely if these warnings are not heeded.

Supplementary information and useful tips.

1.3 Safety information

Applications conforming with specifications

The system is constructed and produced for:

- communication and process control
- general control and automation tasks
- industrial applications
- operation within the environmental conditions specified in the technical data
- installation into a cubicle

DANGER!
This device is not certified for applications in

– in explosive environments (EX-zone)

Documentation

The manual must be available to all personnel in the

- project design department
- installation department
- commissioning
- operation

CAUTION!
The following conditions must be met before using or commissioning the components described in this manual:

– Hardware modifications to the process control system should only be carried out when the system has been disconnected from power!
– Installation and hardware modifications only by properly trained personnel.
– The national rules and regulations of the respective country must be satisfied (installation, safety, EMC ...)

Disposal

National rules and regulations apply to the disposal of the unit!

2 Basics

2.1 Safety information for users

Handling of electrostatic sensitive modules

VIPA modules make use of highly integrated components in MOS-Technology. These components are extremely sensitive to over-voltages that can occur during electrostatic discharges. The following symbol is attached to modules that can be destroyed by electrostatic discharges.

The Symbol is located on the module, the module rack or on packing material and it indicates the presence of electrostatic sensitive equipment. It is possible that electrostatic sensitive equipment is destroyed by energies and voltages that are far less than the human threshold of perception. These voltages can occur where persons do not discharge themselves before handling electrostatic sensitive modules and they can damage components thereby, causing the module to become inoperable or unusable. Modules that have been damaged by electrostatic discharges can fail after a temperature change, mechanical shock or changes in the electrical load. Only the consequent implementation of protection devices and meticulous attention to the applicable rules and regulations for handling the respective equipment can prevent failures of electrostatic sensitive modules.

Shipping of modules

Modules must be shipped in the original packing material.

Measurements and alterations on electrostatic sensitive modules

When you are conducting measurements on electrostatic sensitive modules you should take the following precautions:

- Floating instruments must be discharged before use.
- Instruments must be grounded.

Modifying electrostatic sensitive modules you should only use soldering irons with grounded tips.

CAUTION!
Personnel and instruments should be grounded when working on electrostatic sensitive modules.

2.2 Basics INTERBUS

General

INTERBUS is a pure master/slave system that has very few protocol overheads. For this reason it is well suited for applications on the sensor/actuator level. INTERBUS was developed by PHOENIX CONTACT, Digital Equipment and the Technical University of Lemgo during the 80s. The first system components became available in 1988. To this day the communication protocol has remained virtually unchanged. It is therefore means that it is entirely possible to connect devices of the first generation to the most recent master interfaces (generation 4). INTERBUS devices are subject to the DIN standard 19258 that defines levels 1 and 2 of the protocol amongst others.

INTERBUS as shift register

INTERBUS is based upon a ring structure that operates as a cyclic shift register. Every INTERBUS module inserts a shift register into the ring. The number of I/O points supported by the module determines the length of this shift register.

A ring-based shift register is formed due to the fact that all the devices are connected in series and that the output of the last shift register is returned to the bus master. The length and the structure of this shift register depend on the physical construction of the entire INTERBUS system.

INTERBUS operates by means of a master-slave access method where the master also provides the link to any high-level control system. The ring-structure includes all connected devices actively in a closed communication loop.

In comparison to client-server protocols where data is only exchanged when a client receives a properly addressed command, INTERBUS communications is cyclic in nature and data is exchanged at constant intervals. Every data cycle addresses all devices on the bus.

Restrictions

- Max. 512 participants with 32byte I/O per station
- Up to 400m distance between 2 stations at 500kbyte
- Total distance up to 13km (Repeater function in every station)
- Removal res. addition of modules during runtime is not permitted
- Data consistency is secure for 1byte. To avoid inconsistencies use the *asynchronous* data exchange with consistency bit or the *interrupt controlled* synchronous pulse.

Before alterations you must disconnect the according bus coupler from voltage. Please take care to adjust the initialization in the master when changing the periphery!

Modes of operation

INTERBUS has two modes of operation:

- ID cycle
  - An ID cycle is issued when the INTERBUS system is being initialized and also upon request. During the ID cycle the bus master reads the ID register of every module connected to the bus to generate the process image.
- Data cycle
  - The actual transfer of data occurs during the data cycle. During the data cycle the input data from the registers of all devices is transferred to the master and the output data is transferred from the master to the devices. This is a full duplex data transfer.

ID cycle

During the ID cycle that is executed when the INTERBUS system is being initialized the different modules connected to the bus identify themselves with their individual functionality and the word length. When the INTERBUS coupler is turned on, it determines its INTERBUS length during the initialization phase of the bus modules and generates the

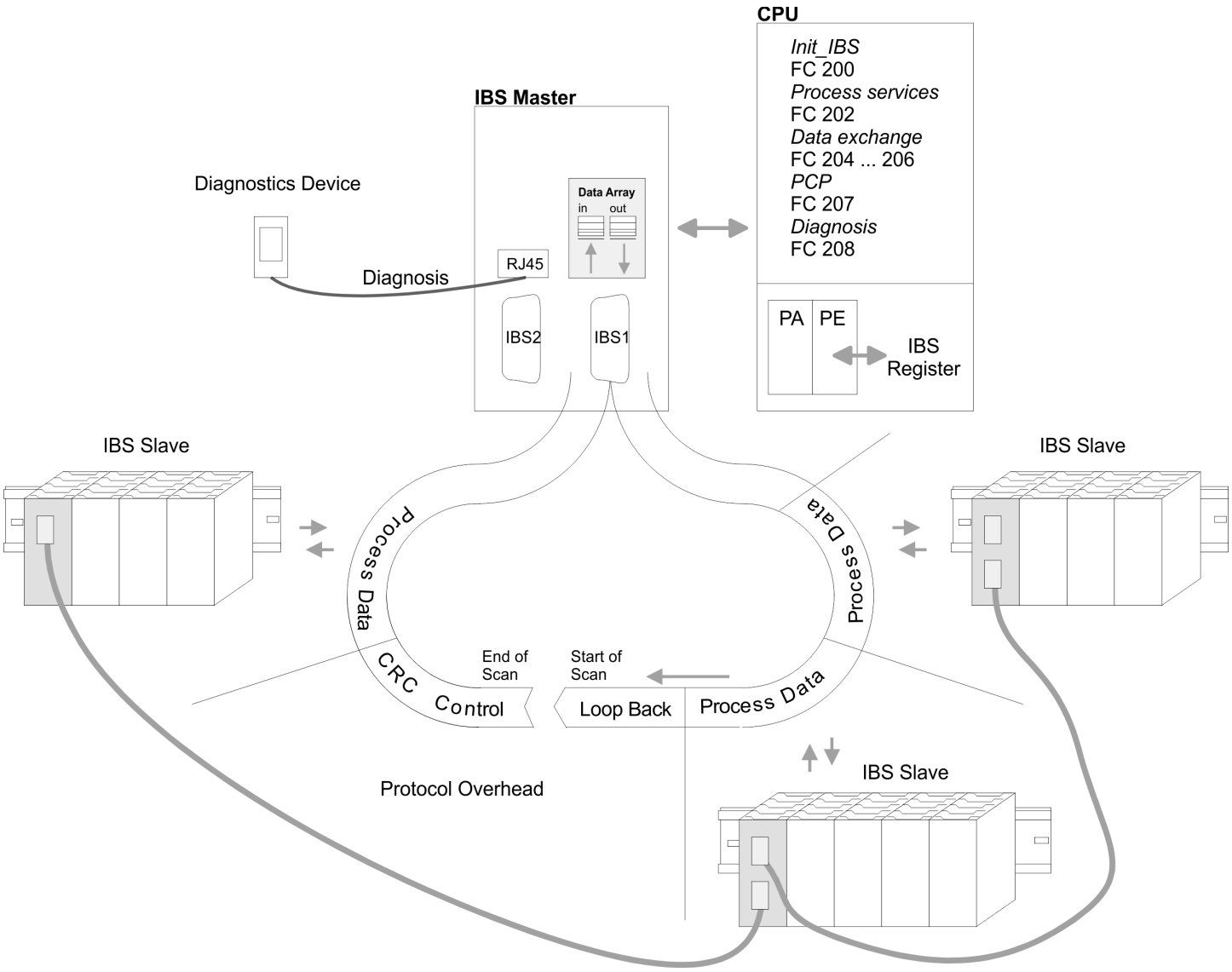
respective ID code. Depending on the configuration the INTERBUS coupler replies with a message identifying it as an analog or a digital remote bus device with variable word length. The INTERBUS ID code consists of 2byte. The MSB (byte 2) describes the length of the data words that will be transferred. The LSB (byte 1) describes the type of bus module, i.e. the type of signal and other performance criteria

MSB

Byte	Bit 7 ... Bit 0
1	■ Bit 1 ... 0: Direction of data transfer: – 00: not used – 01: output – 10: input – 11: input/output ■ Bit 3 ... 2: terminal type ■ Bit 7 ... 4: terminal class The type and class are determined by the INTERBUS-Club
2	■ Bit 4 ... 0: Data width 0 to 10 words (binary) ■ Bit 7 ... 5: reserved

Data cycle

- Process data words also contain control and inspection information. This information is only transferred once at the beginning or at the end of the peripheral data of any data cycle. This is why this system is also referred to as a cumulative frame procedure.
- The communication principle is independent of the type of data being transferred: Process data that must be transferred to the periphery is stored in the output buffer of the master in the same sequence as the output stations are connected to the bus. The transfer occurs when the master shifts the "loop-back word" through the ring. Following the loop-back word, all the output data is placed on the bus. This means that the data is shifted through the shift register. The information from the process is returned as input data to the input buffer of the master at the same time as the output data is being sent.
- The output data is located at the correct position in the shift registers of the different stations when the entire cumulative frame telegram has been sent and read back again. At this point, the master issues a special control command to the devices on the bus to indicate the end of the data transfer cycle.
- When the data check sequence has been processed, output data for the process is transferred from the shift registers. This is stored in the devices connected to the bus and transferred to the respective periphery. At the same time, new information is read from the periphery into the shift registers of the input devices in preparation for the next input cycle.
- This procedure is repeated on a cyclic basis. This means that the input and output buffers of the master are also updated cyclically. INTERBUS data communications is therefore full duplex in nature; i.e. both input data and output data are transferred during a single data cycle.


CPU
Init_IBS
FC 200
Process services
FC 202
Data exchange
FC 204 ... 206
PCP
FC 207
Diagnosis
FC 208
PA
PE
IBS Register
IBS Master
Data Array
in
out
RJ45
IBS2
IBS1
Diagnostics Device
Diagnosis
IBS Slave
IBS Slave
IBS Slave
Process Data
Process Data
CRC
Control
End of Scan
Start of Scan
Loop Back
Process Data
Protocol Overhead

2.3 General data

Conformity and approval		
Conformity		
CE	2014/35/EU	Low-voltage directive
	2014/30/EU	EMC directive
Approval		
UL		Refer to Technical data
others		
RoHS	2011/65/EU	Restriction of the use of certain hazardous substances in electrical and electronic equipment

Protection of persons and device protection		
Type of protection	-	IP20
Electrical isolation		
to the field bus	-	electrically isolated
to the process level	-	electrically isolated
Insulation resistance		-
Insulation voltage to reference earth		
Inputs / outputs	-	AC / DC 50V, test voltage AC 500V
Protective measures	-	against short circuit

Environmental conditions to EN 61131-2		
Climatic		
Storage / transport	EN 60068-2-14	-25…+70°C
Operation		
Horizontal installation hanging	EN 61131-2	0…+60°C
Horizontal installation lying	EN 61131-2	0…+55°C
Vertical installation	EN 61131-2	0…+50°C
Air humidity	EN 60068-2-30	RH1 (without condensation, rel. humidity 10…95%)
Pollution	EN 61131-2	Degree of pollution 2
Installation altitude max.	-	2000m
Mechanical		
Oscillation	EN 60068-2-6	1g, 9Hz ... 150Hz
Shock	EN 60068-2-27	15g, 11ms

General data

Mounting conditions		
Mounting place	-	In the control cabinet
Mounting position	-	Horizontal and vertical

EMC	Standard		Comment
Emitted interference	EN 61000-6-4		Class A (Industrial area)
Noise immunity zone B	EN 61000-6-2		Industrial area
		EN 61000-4-2	ESD 8kV at air discharge (degree of severity 3), 4kV at contact discharge (degree of severity 2)
		EN 61000-4-3	HF field immunity (casing) 80MHz … 1000MHz, 10V/m, 80% AM (1kHz) 1.4GHz ... 2.0GHz, 3V/m, 80% AM (1kHz) 2GHz ... 2.7GHz, 1V/m, 80% AM (1kHz)
		EN 61000-4-6	HF conducted 150kHz … 80MHz, 10V, 80% AM (1kHz)
		EN 61000-4-4	Burst, degree of severity 3
		EN 61000-4-5	Surge, degree of severity 3 *

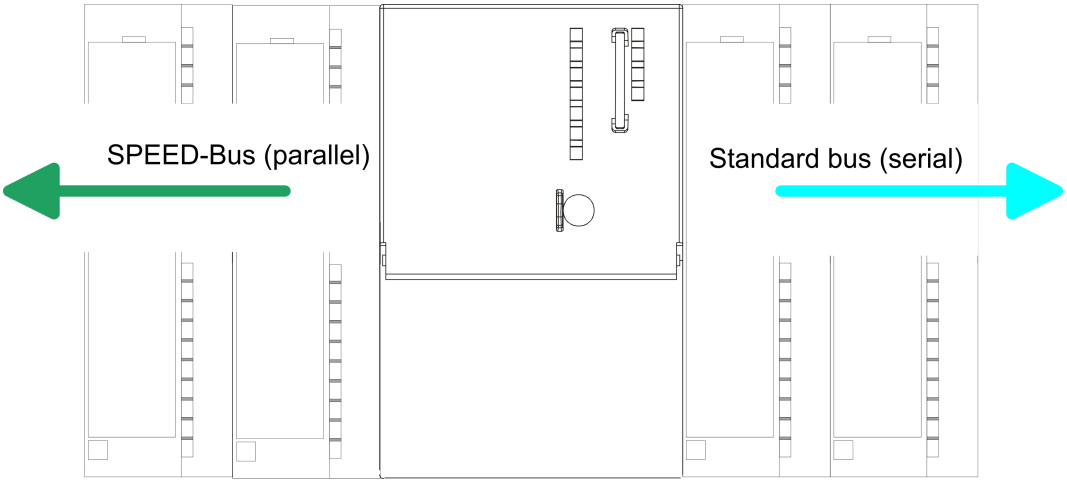
*) Due to the high-energetic single pulses with Surge an appropriate external protective circuit with lightning protection elements like conductors for lightning and overvoltage is necessary.

3 Assembly and installation guidelines

3.1 Overview

SPEED-Bus

- The SPEED-Bus is a 32bit parallel bus developed from VIPA.
- Via the SPEED-Bus you may connect up to 10 SPEED-Bus modules to your CPU.
- In opposite to the "standard" backplane bus where the modules are plugged-in at the right side of the CPU by means of single bus connectors, the modules at the SPEED-Bus are plugged-in at the left side of the CPU via a special SPEED-Bus rail.
- VIPA delivers profile rails with integrated SPEED-Bus for 2, 6, or 10 SPEED-Bus peripheral modules with different lengths.
- Each SPEED-Bus rail has a slot for an external power supply. This allows you to raise the maximum current at the back plane bus. Only the "SLOT1 DCDC" allows you to plug-in either a SPEED-Bus module or an additional power supply (307-1FB70).



SPEED-Bus peripheral modules

The SPEED-Bus peripheral modules may exclusively plugged at the SPEED-Bus slots at the left side of the CPU. The following SPEED-Bus modules are in preparation:

- Fast fieldbus modules like PROFIBUS DP, Interbus, CANopen master and CANopen slave
- Fast CP 343 (CP 343 Communication processor for Ethernet)
- Fast CP 341 with double RS 422/485 interface
- Fast digital input-/output modules (Fast Digital IN/OUT)

Serial Standard bus

The single modules are directly installed on a profile rail and connected via the backplane bus coupler. Before installing the modules you have to clip the backplane bus coupler to the module from the backside. The backplane bus couplers are included in the delivery of the peripheral modules.

Parallel SPEED-Bus

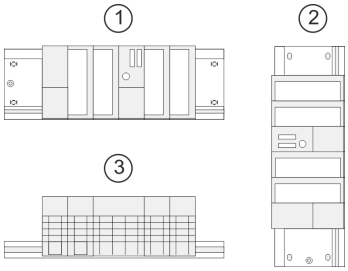
With SPEED-Bus the bus connection happens via a SPEED-Bus rail integrated in the profile rail at the left side of the CPU. Due to the parallel SPEED-Bus not all slots must be occupied in sequence.

SLOT 1 for additional power supply

At slot (SLOT 1 DCDC) you may plug either a SPEED-Bus module or an additional power supply.

Assembly possibilities

You may assemble the System 300 horizontally, vertically or lying. Please regard the allowed environment temperatures:



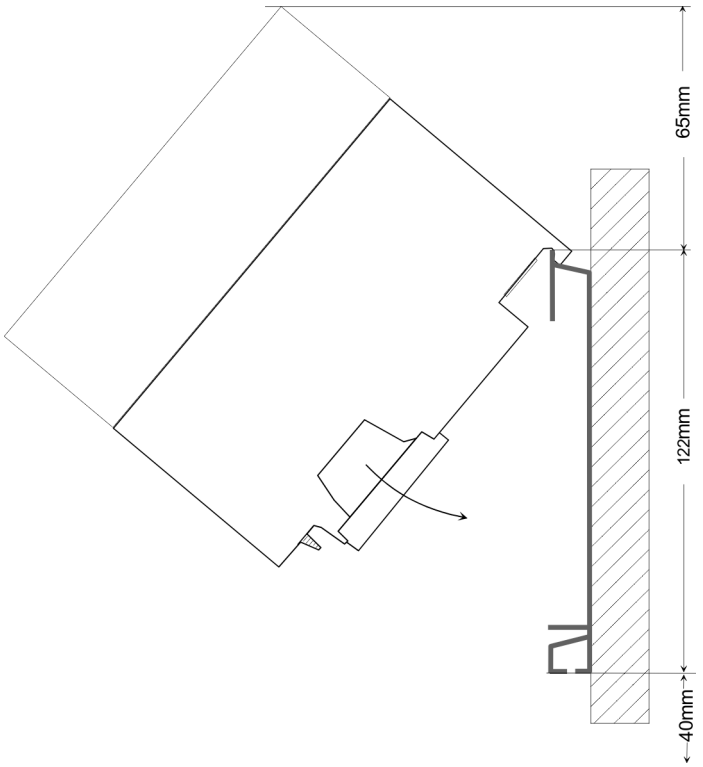
1 horizontal assembly: from 0 to 60°C
2 vertical assembly: from 0 to 50°C
3 lying assembly: from 0 to 55°C

3.2 Installation dimensions

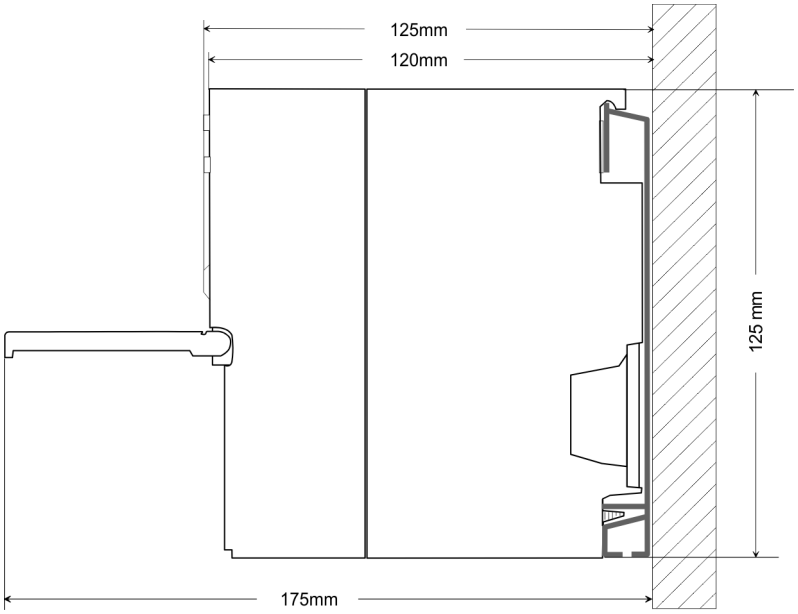
Dimensions Basic enclosure

1tier width (WxHxD) in mm: 40 x 125 x 120

Dimensions



Installation dimensions



3.3 Assembly SPEED-Bus

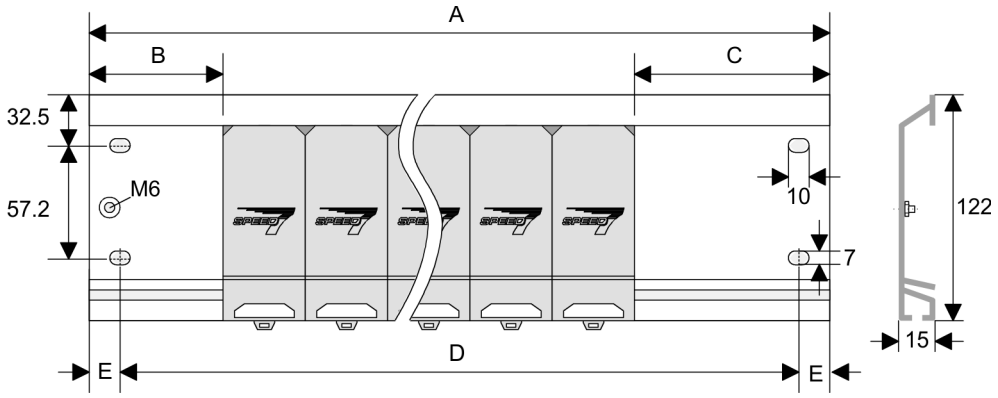
Pre-manufactured SPEED-Bus profile rail

For the deployment of SPEED-Bus modules, a pre-manufactured SPEED-Bus rail is required. This is available mounted on a profile rail with 2, 6 or 10 extension slots.

Dimensions

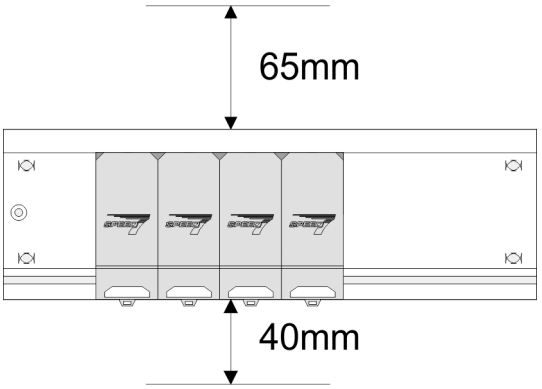
Order number	Number of modules SPEED-Bus/Standard bus	A	B	C	D	E
391-1AF10	2/6	530	100	268	510	10
391-1AF30	6/2	530	100	105	510	10
391-1AF50	10/0	530	20	20	510	10
391-1AJ10	2/15	830	22	645	800	15
391-1AJ30	6/11	830	22	480	800	15
391-1AJ50	10/7	830	22	320	800	15

Measures in mm

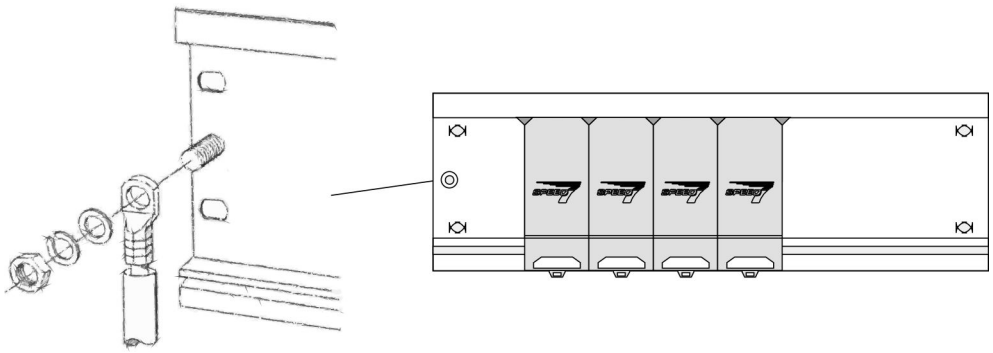


Installation of the profile rail

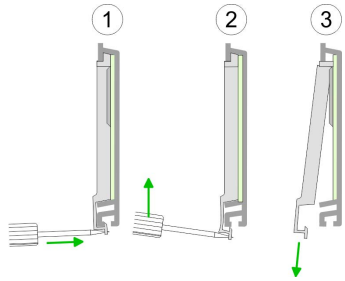
1. Bolt the profile rail with the background (screw size: M6), so that you still have minimum 65mm space above and 40mm below the profile rail. Please look for a low-impedance connection between profile rail and background.



2. Connect the profile rail with the protected earth conductor. The minimum cross-section of the cable to the protected earth conductor has to be 10mm^2.

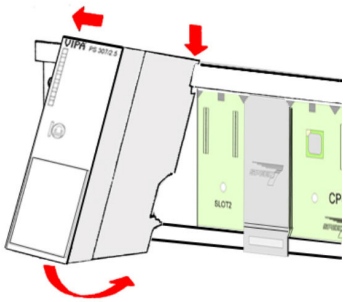


Installation SPEED-Bus module

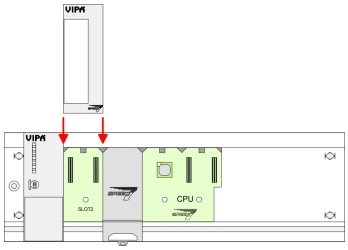


1. Dismantle the according protection flaps of the SPEED-Bus slot with a screw driver (open and pull down).

   For the SPEED-Bus is a parallel bus, not every SPEED-Bus slot must be used in series. Leave the protection flap installed at an unused SPEED-Bus slot.

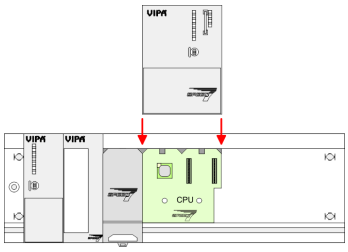


2. At deployment of a DC 24V power supply, install it at the shown position at the profile rail at the left side of the SPEED-Bus and push it to the left to the isolation bolt of the profile rail.
3. Fix the power supply by screwing.

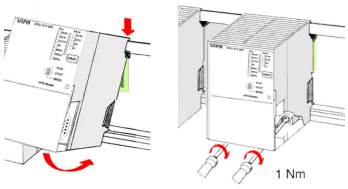


4. To connect the SPEED-Bus modules, plug it between the triangular positioning helps to a slot marked with "SLOT ..." and pull it down.
5. Only the "SLOT1 DCDC" allows you to plug-in either a SPEED-Bus module or an additional power supply.
6. Fix the CPU by screwing.

Installation CPU without Standard-Bus-Modules

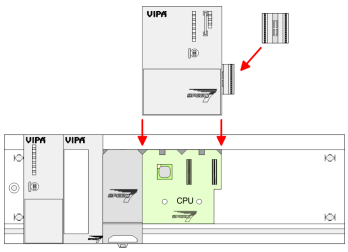


1. To deploy the SPEED7-CPU exclusively at the SPEED-Bus, plug it between the triangular positioning helps to the slot marked with "CPU SPEED7" and pull it down.

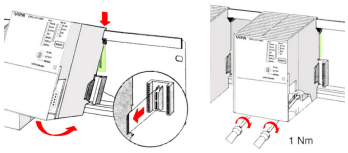


2. Fix the CPU by screwing.

Installation CPU with Standard-Bus-Modules

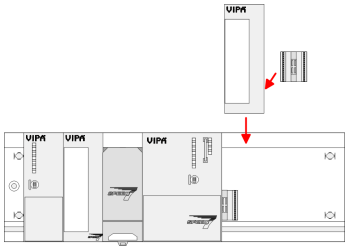


1. If also standard modules shall be plugged, take a bus coupler and click it at the CPU from behind like shown in the picture. Plug the CPU between the triangular positioning helps to the slot marked with "CPU SPEED7" and pull it down.



2. Fix the CPU by screwing.

Installation Standard-Bus-Modules



Repeat this procedure with the peripheral modules, by clicking a backplane bus coupler, stick the module right from the modules you've already fixed, click it downwards and connect it with the backplane bus coupler of the last module and bolt it.

CAUTION!

- The power supplies must be released before installation and repair tasks, i.e. before handling with the power supply or with the cabling you must disconnect current/voltage (pull plug, at fixed connection switch off the concerning fuse)!
- Installation and modifications only by properly trained personnel!

3.4 Installation guidelines

General

The installation guidelines contain information about the interference free deployment of a PLC system. There is the description of the ways, interference may occur in your PLC, how you can make sure the electromagnetic compatibility (EMC), and how you manage the isolation.

What does EMC mean?

Electromagnetic compatibility (EMC) means the ability of an electrical device, to function error free in an electromagnetic environment without being interfered respectively without interfering the environment.

The components of VIPA are developed for the deployment in industrial environments and meets high demands on the EMC. Nevertheless you should project an EMC planning before installing the components and take conceivable interference causes into account.

Possible interference causes

Electromagnetic interferences may interfere your control via different ways:

- Electromagnetic fields (RF coupling)
- Magnetic fields with power frequency
- Bus system
- Power supply
- Protected earth conductor

Depending on the spreading medium (lead bound or lead free) and the distance to the interference cause, interferences to your control occur by means of different coupling mechanisms.

There are:

- galvanic coupling
- capacitive coupling
- inductive coupling
- radiant coupling

Basic rules for EMC

In the most times it is enough to take care of some elementary rules to guarantee the EMC. Please regard the following basic rules when installing your PLC.

- Take care of a correct area-wide grounding of the inactive metal parts when installing your components.
  - Install a central connection between the ground and the protected earth conductor system.
  - Connect all inactive metal extensive and impedance-low.
  - Please try not to use aluminium parts. Aluminium is easily oxidizing and is therefore less suitable for grounding.
- When cabling, take care of the correct line routing.
  - Organize your cabling in line groups (high voltage, current supply, signal and data lines).
  - Always lay your high voltage lines and signal respectively data lines in separate channels or bundles.
  - Route the signal and data lines as near as possible beside ground areas (e.g. suspension bars, metal rails, tin cabinet).

- Proof the correct fixing of the lead isolation.
  - Data lines must be laid isolated.
  - Analog lines must be laid isolated. When transmitting signals with small amplitudes the one sided laying of the isolation may be favourable.
  - Lay the line isolation extensively on an isolation/protected earth conductor rail directly after the cabinet entry and fix the isolation with cable clamps.
  - Make sure that the isolation/protected earth conductor rail is connected impedance-low with the cabinet.
  - Use metallic or metallised plug cases for isolated data lines.
- In special use cases you should appoint special EMC actions.
  - Consider to wire all inductivities with erase links.
  - Please consider luminescent lamps can influence signal lines.
- Create a homogeneous reference potential and ground all electrical operating supplies when possible.
  - Please take care for the targeted employment of the grounding actions. The grounding of the PLC serves for protection and functionality activity.
  - Connect installation parts and cabinets with your PLC in star topology with the isolation/protected earth conductor system. So you avoid ground loops.
  - If there are potential differences between installation parts and cabinets, lay sufficiently dimensioned potential compensation lines.

Isolation of conductors

Electrical, magnetically and electromagnetic interference fields are weakened by means of an isolation, one talks of absorption. Via the isolation rail, that is connected conductive with the rack, interference currents are shunt via cable isolation to the ground. Here you have to make sure, that the connection to the protected earth conductor is impedance-low, because otherwise the interference currents may appear as interference cause.

When isolating cables you have to regard the following:

- If possible, use only cables with isolation tangle.
- The hiding power of the isolation should be higher than 80%.
- Normally you should always lay the isolation of cables on both sides. Only by means of the both-sided connection of the isolation you achieve high quality interference suppression in the higher frequency area. Only as exception you may also lay the isolation one-sided. Then you only achieve the absorption of the lower frequencies. A one-sided isolation connection may be convenient, if:
  - the conduction of a potential compensating line is not possible.
  - analog signals (some mV respectively µA) are transferred.
  - foil isolations (static isolations) are used.
- With data lines always use metallic or metallised plugs for serial couplings. Fix the isolation of the data line at the plug rack. Do not lay the isolation on the PIN 1 of the plug bar!
- At stationary operation it is convenient to strip the insulated cable interruption free and lay it on the isolation/protected earth conductor line.
- To fix the isolation tangles use cable clamps out of metal. The clamps must clasp the isolation extensively and have well contact.
- Lay the isolation on an isolation rail directly after the entry of the cable in the cabinet. Lead the isolation further on to your PLC and don't lay it on there again!

CAUTION!

Please regard at installation!

At potential differences between the grounding points, there may be a compensation current via the isolation connected at both sides.

Remedy: Potential compensation line

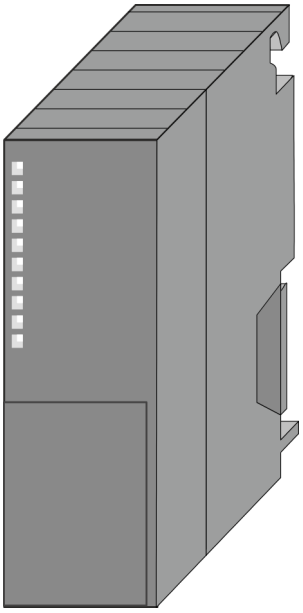
4 Hardware description

4.1 Properties

CP 342-2IA71

The CP CP 342S-2IBS in the following may only be used at the SPEED-Bus.

- Dual **I**NTER**BUS** master (IBS master) for SPEED-Bus.
- Up to 512 slaves connectable.
- Supports PCP communication 2.0 with bandwidths of 1, 2 and 4 words at 62 couplers with basic functions and 127 configurable couplers.
- Diagnostics via LEDs, diagnostics device (342-0IA01) and DPM **d**ual **p**ort **m**emory.



Order data

Type	Order No.	Description
CP 342S-2IBS	342-2IA71	Dual INTERBUS master for SPEED-Bus
IBS-Diag	342-0IA01	Diagnostics device with RJ45 plug for VIPA INTERBUS master

4.2 Structure

INTERBUS platform

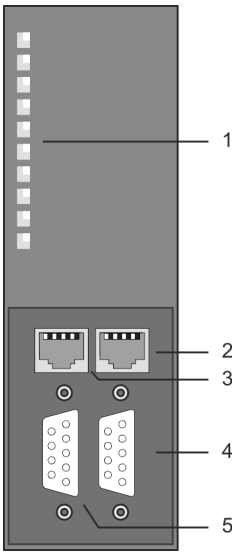
As INTERBUS hardware platform, 2 INTERBUS master cards USC4-2 from Phoenix Contact are used. The INTERBUS section manages every task concerning network management and diagnostics. Here the communication with the CPU happens via a **D**ual **p**ort **m**emory (DPM).

Among others, the DPM has the following interfaces for send and receive:

- SSGI (**S**tandard **S**ignal **I**nterface) for the exchange of messages like e.g. request of services from the master
- DTA (**D**a**t**a) interface for the exchange of process data

Due to the fact that VIPA provides the same services for master and slave parameterization for this master, we refer at the according places to the extensive documentation of the services from Phoenix Contact.

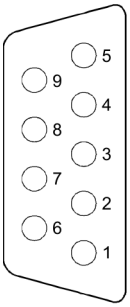
CP 342-2IA71



1 LEDs status indicators
The following components are under the front flap
2 RJ45 jack to connect diagnostics device to IBS1
3 RJ45 jack to connect diagnostics device to IBS2
4 RS422 INTERBUS interface IBS1
5 RS422 INTERBUS interface IBS2

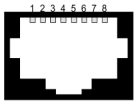
Interfaces

IBS1/IBS2
RS422
X2/X3



① DOH
② DIH
③ GND (ISO)
④ GND
⑤ +5V (ISO)
⑥ DOL
⑦ DIL
⑧ +5V
⑨ reserved

2x RJ45
Diagnostic device



① GND
② PCS3
③ MISO
④ MOSI
⑤ SCK
⑥ PCS2
⑦ VCC
⑧ n. c.

Power supply

The CP 342-2IA71 gets its power supply via the SPEED-Bus.

Chapter 4.3 'Technical data' on page 26

RJ45 diagnostics jack

For each INTERBUS master part there is a RJ45 jack below the front flap to connect the VIPA diagnostics device with order number: 342-0IA01.

8pin RJ45 jack:

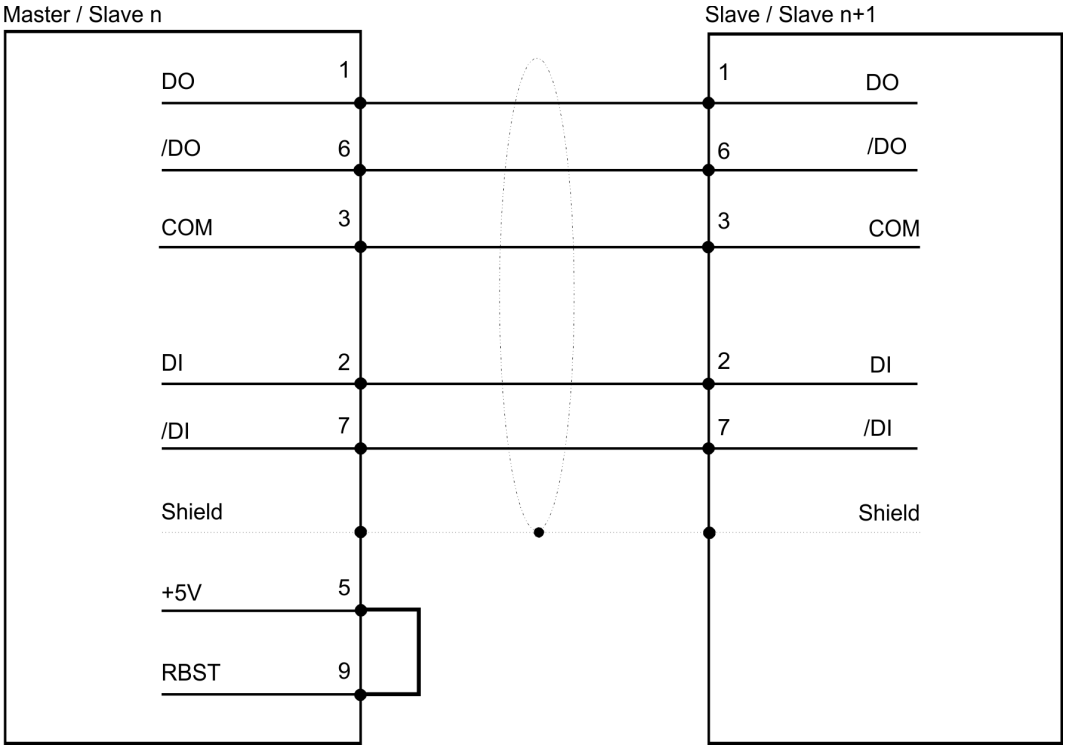
Pin	Signal	Meaning
1	GND	Ground
2	PCS3	Chip select 3
3	MISO	Serial data input
4	MOSI	Serial data output
5	SCK	Clock
6	PCS2	Chip select 2
7	VCC	5V
8	n.c.	not connected

RS422 Interbus jack

The interfaces RS422 for each IBS master for the Interbus connections are located on the front flap of the module. Although Interbus is substantial build-up in line structure (only one line from the master to the last module) it is in principle a ring structure where the for- and backwards conductor are together in one lead. The ring is closed by the last participant. The most devices are closing the ring automatically when no continuative lead is connected. For master-slave and slave-slave connection the same connection cable is used. Due to the ring structure and the common logic ground, the cable consists of 5 cores and has the following assignment:

9pin D-type jack (IBS 1 and IBS 2):

Pin	Assignment
1	DOH
2	DIH
3	GND_{iso}
4	GND
5	$+5V_{iso}$ (90mA)
6	DOL
7	DIL
8	+5V (90mA)
9	reserved



Please take care that the plug for the „continuative interface" has a bridge between Pin 5 and 9, otherwise the following slaves are not recognized!

Isolation

For Interbus distant bus segments cover a wide volume expansion, the single segments must be isolated to avoid potential procrastination. According to the recommendation of the Interbus-Club, an isolation of the incoming distant bus interface from the rest of the system is sufficient. The continuative distant bus interface is thus at the potential of the rest of the system and the backplane bus. Please use metal plug casings and put the cable screen on the plug casing.

Hinweis

When use the CP 342-2IA71, the digital fast output module 322-1BH70 (DO 16xDC 24V 0,5A) is not allowed.

LEDs

The CP 342-2IA71 carries at each INTERBUS interface a number of LEDs that are available for diagnostic purposes on the bus and for displaying the local status. These give information according to the following pattern over the operating condition of the CP:

RUN green	ERR red	BSA yellow	PF yellow	HF yellow	Meaning
☐	☐	☐	☐	☐	Module is not power supplied
■	☐	☐	☐	☐	INTERBUS is ready for data transfer
◪	☐	☐	☐	☐	INTERBUS is active, bus parameters are transferred, bus is checked.
◪	■	☐	☐	☐	At least 1 slave is missing or bus error.
◪	■	■	☐	☐	At least 1 segment of the subordinate bus is switched off.
■	■	☐	■	☐	Peripheral fault at a subordinate bus member
☐	■	☐	☐	■	Error in CP 342-2IA71
flashing: ◪					

4.3 Technical data

Order no.	342-2IA71
Type	CP 342S IBS, dual INTERBUS master SPEED-Bus
SPEED-Bus	✓
Current consumption/power loss	
Current consumption from backplane bus	1 A
Power loss	4.5 W
Status information, alarms, diagnostics	
Status display	yes
Interrupts	no
Process alarm	no
Diagnostic interrupt	no
Diagnostic functions	no
Diagnostics information read-out	none
Supply voltage display	yes
Group error display	yes
Channel error display	none
Functionality Sub-D interfaces	
Type	X2
Type of interface	RS422
Connector	Sub-D, 9-pin, female
Electrically isolated	✓
MPI	-
MP²I (MPI/RS232)	-
Point-to-point interface	-
5V DC Power supply	max. 90mA isolated and max. 90mA non-isolated
24V DC Power supply	-
Type	X3
Type of interface	RS422
Connector	Sub-D, 9-pin, female
Electrically isolated	✓
MPI	-
MP²I (MPI/RS232)	-
Point-to-point interface	-
5V DC Power supply	max. 90mA isolated and max. 90mA non-isolated
24V DC Power supply	-

Order no.	342-2IA71
Functionality RJ45 interfaces	
Type	DIAG 1
Type of interface	-
Connector	RJ45
Electrically isolated	-
PG/OP channel	-
Number of connections, max.	-
Productive connections	-
Fieldbus	-
Type	DIAG 2
Type of interface	-
Connector	RJ45
Electrically isolated	-
PG/OP channel	-
Number of connections, max.	-
Productive connections	-
Fieldbus	-
Housing	
Material	PPE
Mounting	DIN rail SPEED-Bus
Mechanical data	
Dimensions (WxHxD)	40 mm x 125 mm x 120 mm
Net weight	260 g
Weight including accessories	-
Gross weight	-
Environmental conditions	
Operating temperature	0 °C to 60 °C
Storage temperature	-25 °C to 70 °C
Certifications	
UL certification	-
KC certification	-

5 Deployment

5.1 Fast introduction

Overview

The integration of the CP into your SPS system should take place with the following proceeding:

- Assembly and commissioning
- Hardware configuration (integration CP in CPU)
- Communication with the user program

Assembly and commissioning

1. Install your SPEED-Bus system with a SPEED7 CPU and a 342-2IA71
2. Wire-up the system. A detailed description about this may be found in the chapter "Assembly and installation guidelines".
3. Switch power ON.
   ⇨ After a short boot time the CP is in the system.
4. Start the Siemens SIMATIC manager with an online connection to the CPU. More about this may be found in the manual of the CPU.

For the deployment of the System 300S modules at the SPEED-Bus you have to include the System 300S modules into the hardware catalog via the GSD-file SPEEDBUS.GSD from VIPA.

Hardware configuration

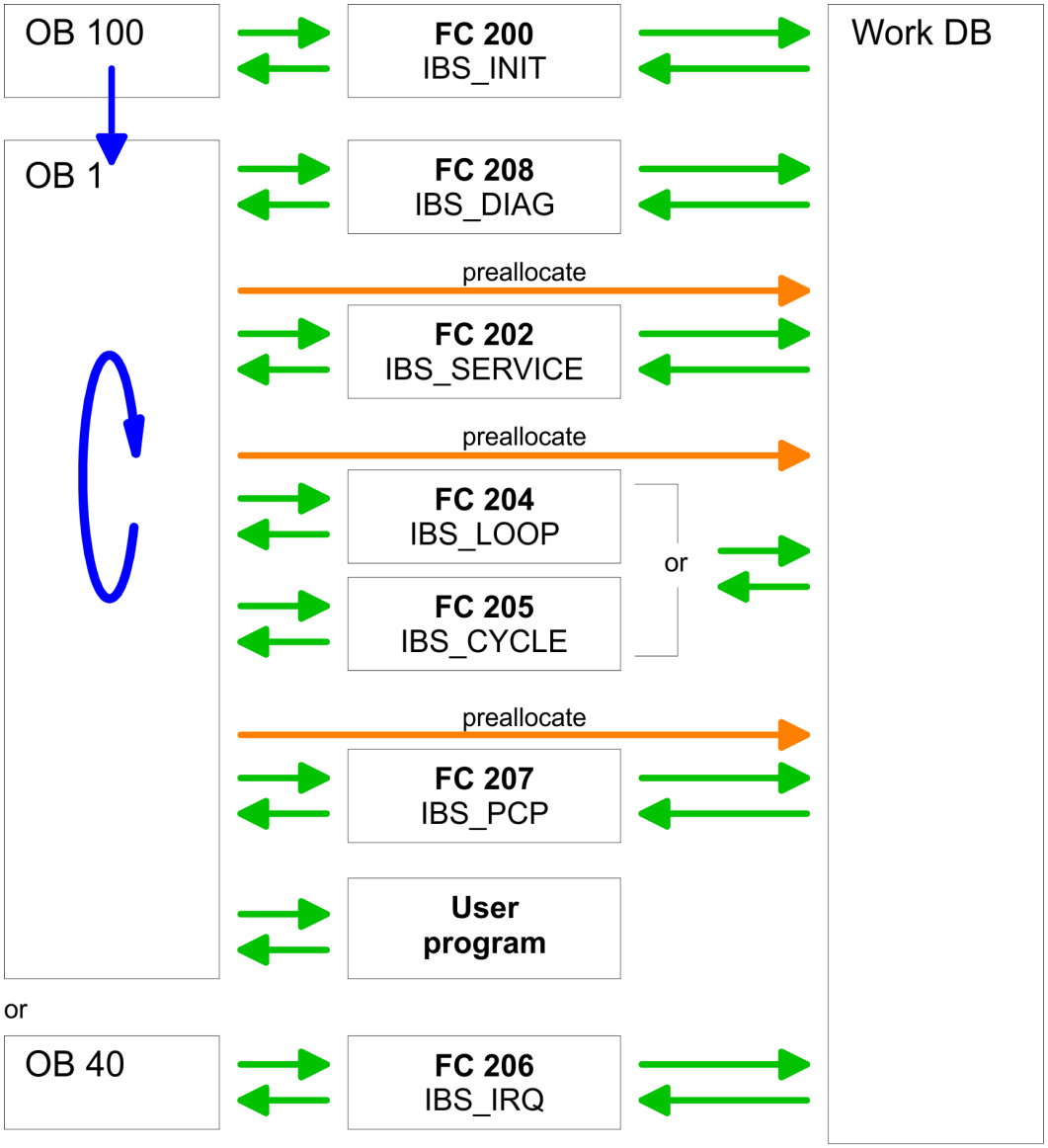
1. Install the SPEEDBUS.GSD from VIPA.
2. For hardware configuration jump within your project to the hardware configurator of the Siemens SIMATIC manager.
3. Insert a profile rail
4. Place the appropriate Siemens CPU at slot 2 and parameterize the CPU if necessary.
5. If there are modules at the standard bus right beside the CPU and parameterize the modules if necessary.

The project engineering of the SPEED-Bus modules happens by means of a virtual Profibus DP master system. For this, place as last module a DP master (342-5DA02 V5.0) with master system.

1. To this master system you assign every SPEED-Bus module e.g. IBS master as VIPA_SPEEDBUS slave.
2. Set as Profibus address the slot no. (100...110) of the module and place the according module from the hardware catalog of VIPA_SPEEDBUS to slot 0 of the slave system.
3. In this way place the SPEED-Bus CP 342-2IA71. In the hardware catalog is a CP 342-2IA71 at VIPA_SPEEDBUS available.

Communication with the user program

For the processing of the connecting jobs at PLC side a user program is necessary in the CPU. Here VIPAspecific blocks are to be used. These blocks may be found at Service area at www.vipa.com. Please regard for each of the IBS master you have to create a work DB. The user program should have the following structure:



5.2 Addressing at SPEED-Bus

Overview

To provide specific addressing of the installed peripheral modules, certain addresses must be allocated in the CPU. With no hardware configuration present, the CPU assigns automatically peripheral I/O addresses during boot procedure depending on the plug-in location amongst others also for plugged modules at the SPEED-Bus.

Maximal pluggable modules

In the hardware configurator from Siemens up to 8 modules per row may be parameterized. At deployment of SPEED7 CPUs up to 32 modules at the standard bus and 10 further modules at the SPEED-Bus may be controlled. CPs and DP masters that are additionally virtual configured at the standard bus are taken into the sum of 32 modules at the standard bus. For the project engineering of more than 8 modules you may use virtual line interface connections. For this you set in the hardware configurator the module IM 360 from the hardware catalog to slot 3 of your 1. profile rail. Now you may extend your system with up to 3 profile rails by starting each with an IM 361 from Siemens at slot 3.

Define addresses by hardware configuration

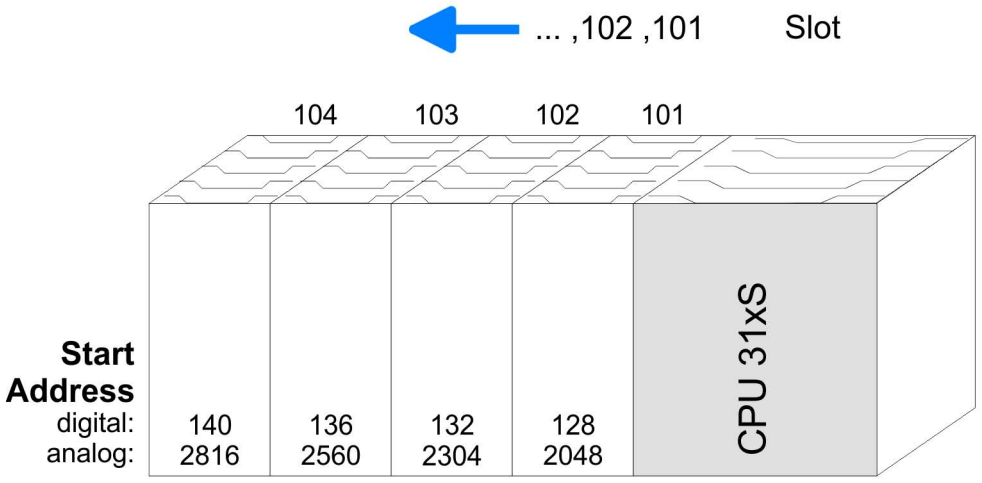
You may access the modules with read res. write accesses to the peripheral bytes or the process image. To define addresses a hardware configuration via a virtual PROFIBUS system by including the SPEEDBUS.GSD may be used. For this, click on the properties of the according module and set the wanted address.

Automatic addressing

If you do not like to use a hardware configuration, an automatic addressing comes into force. At the automatic address allocation DIOs are mapped depending on the slot location with a distance of 4byte and AIOs, FMs, CPs with a distance of 256byte.

Depending on the slot location the start address from where on the according module is stored in the address range is calculated with the following formulas:

- DIOs: Start address = 4×(slot -101)+128
- AIOs, FMs, CPs: Start address = 256×(slot -101)+2048



5.3 Hardware configuration

Preconditions

The hardware configurator is part of the Siemens SIMATIC manager and it serves the project engineering. The modules that may configured here are listed in the hardware catalog. For the deployment of the System 300S modules at the SPEED-Bus you have to include the System 300S modules into the hardware catalog via the GSD-file SPEEDBUS.GSD from VIPA.

For the project engineering a thorough knowledge of the Siemens SIMATIC manager and the hardware configurator from Siemens is required!

Installation of the SPEEDBUS.GSD

The GSD (Geräte-Stamm-Datei) is online available in the following language versions. Further language versions are available on inquires:

Name	Language
SPEEDBUS.GSD	German (default)
SPEEDBUS.GSG	German
SPEEDBUS.GSE	English

The GSD files may be found at www.vipa.com at the service area.

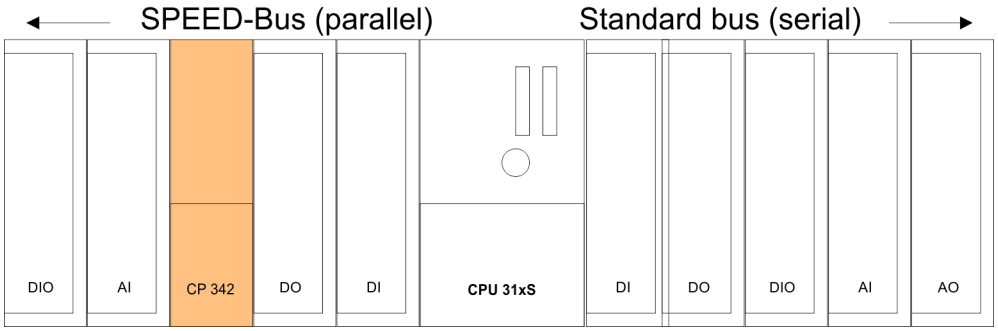
The integration of the SPEEDBUS.GSD takes place with the following proceeding:

1. Go to the service area of www.vipa.com.
2. Load from the download area at *'Config files ➔ PROFIBUS'* the according file for your System 300S.
3. Extract the file to your work directory.
4. Start the hardware configurator from Siemens.
5. Close every project.
6. Select *'Options ➔ Install new GSD-file'*.
7. Navigate to the directory VIPA_System_300S and select **SPEEDBUS.GSD** an.
   ⇨ The SPEED7 CPUs and modules of the System 300S from VIPA may now be found in the hardware catalog at PROFIBUS-DP / Additional field devices / I/O / VIPA_SPEEDBUS.

5.3.1 Steps of project engineering

The following text describes the approach of the project engineering of the CP for SPEED-Bus in the hardware configurator from Siemens at an abstract sample. The project engineering is separated into the following parts:

- Project engineering standard bus
- Project engineering SPEED-Bus as virtual PROFIBUS network

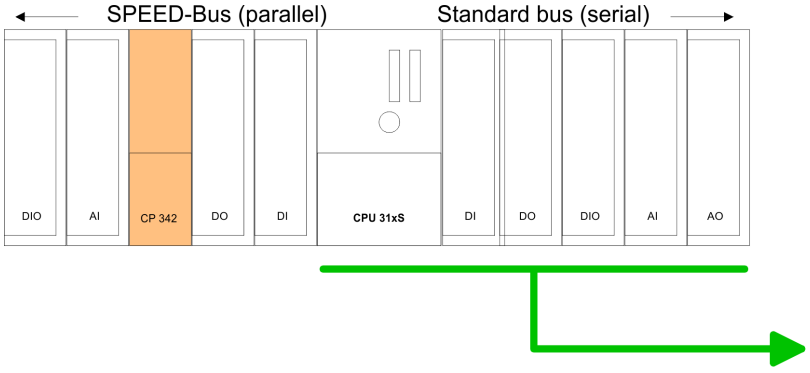


Project engineering of the modules at the standard bus

1. Start the hardware configurator from Siemens with a new project and insert a profile rail from the hardware catalog.
2. Place the corresponding Siemens CPU at slot 2.
3. Parameterize the CPU where appropriate. The parameter window opens by a double click on the according module.

If there are modules at the standard bus right beside the CPU, these are configured with the following approach:

1. Include your System 300 modules at the standard bus in the plugged sequence starting with slot 4.
2. Parameterize the modules where appropriate. The parameter window opens by a double click on the according module.
3. Since as many as 32 modules may be addressed by the SPEED7 CPU in one row, but only 8 modules are supported by the Siemens SIMATIC manager, the IM 360 of the hardware catalog can be used as a virtual bus extension during project engineering. Here 3 further extension racks can be virtually connected via the IM 361. Bus extensions are always placed at slot 3.



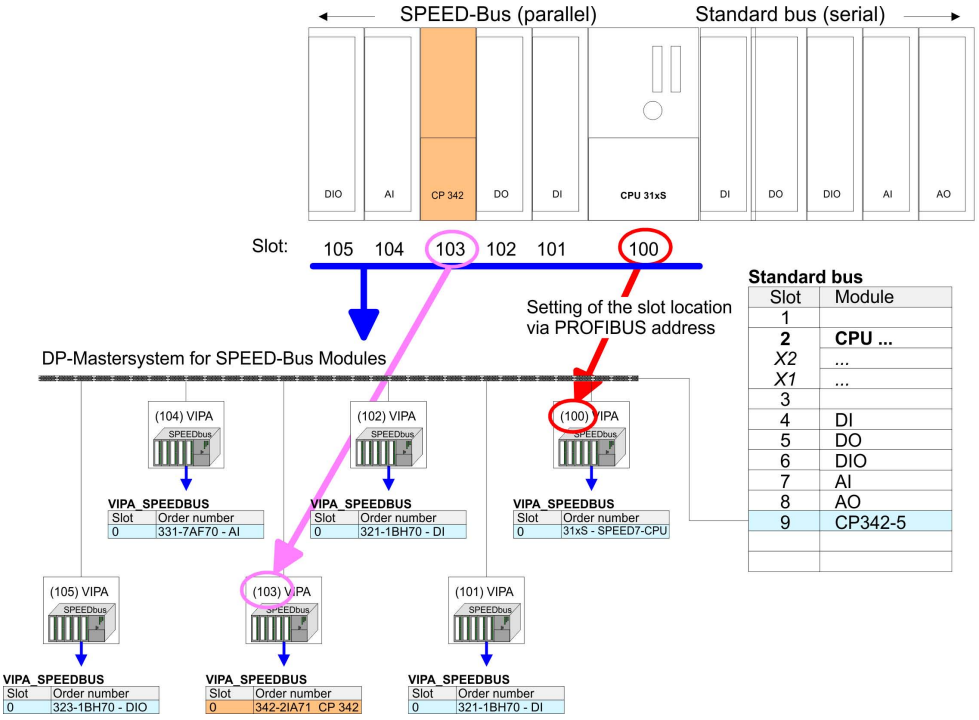
Standard bus

Slot	Module
1	
2	**CPU ...**
X...	...
X...	...
3	
4	DI
5	DO
6	DIO
7	AI
8	AO

5.4 Project engineering SPEED-Bus as virtual PROFIBUS network

The project engineering of the SPEED-Bus modules happens by means of a virtual PROFIBUS DP master system.

1. For this, place as last module a DP master (342-5DA02 V5.0) with master system.
2. For the deployment of the System 300S modules at the SPEED-Bus the inclusion of the System 300S modules into the hardware catalog via the GSD-file SPEEDBUS.GSD from VIPA is required.
3. After the installation of the SPEEDBUS.GSD you may locate at *Profibus DP / Additional field devices / I/O / VIPA_SPEEDBUS* the DP slave system VIPA_SPEEDBUS.
4. Now include for the CPU and every module at the SPEED-Bus a slave system "VIPA_SPEEDBUS". Set as Profibus address the slot no. (100...110) of the module and place the according module from the hardware catalog of VIPA_SPEEDBUS to slot 0 of the slave system.
5. In this way place the SPEED-Bus CP 342-2IA71. In the hardware catalog VIPA_SPEEDBUS a CP 342-2IA71 is available.



- The according module is to be taken over from the HW Catalog of VIPA_SPEEDBUS to slot 0.

5.4.1 Properties CP 342-2IA71

The properties of the CP may be accessed by a double click at the CP 342-2IA71 within your project in the hardware configurator. Every parameter of the CP may be accessed by the registers *Address/ID* and *Parameter Assignment*.

Address/ID

Output Input

By presetting a start address for the input respectively output area the beginning of the address area of the CPU may be determined, which is mapped by the module. Please regard that the base address for input and output are identical. The module occupies 68byte. Here each IBS master part occupies 34byte. The corresponding address value is necessary for integration in the user program. To access the IBS2 master you have to add 34 to the respective address value.

Parameter Assignment

Offset IO address

By presetting the offset address, the addresses entered at Address/ID are incremented with this offset value. So the CP module may be mapped to an address area, which may not be reached during configuration by the Siemens SIMATIC manager. System dependent address overlaps may not be recognized.

5.5 Register allocation

***LADDR* of IBS1 and IBS2**

The structure of the INTERBUS master register is shown at the following table. To access the register of IBS1 for *LADDR* the preset address of the hardware configuration is to be used. To access the IBS2 you have to add to *LADDR* of IBS1 34byte.

Overview

Address	Assignment	Direction
LADDR	Interrupt register	CPU > Master
LADDR+1	Interrupt register	Master > CPU
LADDR+2	SSGI acknowledge	Master > CPU
LADDR+4	SSGI notification	Master > CPU
LADDR+6	SSGI result	Master > CPU
LADDR+8	SSGI status	Master > CPU
LADDR+10	SSGI start	CPU > Master
LADDR+12	reserved	-
LADDR+14	Standard function parameter register	CPU > Master
LADDR+16	Standard function start register	CPU > Master
LADDR+18	Standard function status register	Master > CPU
LADDR+20	Master diagnosis parameter register	Master > CPU
LADDR+22	Master diagnosis status register	Master > CPU
LADDR+24	reserved	-
LADDR+26	Slave diagnosis status register	Master > CPU
LADDR+28	Configuration register	Master > CPU

Address	Assignment	Direction
LADDR+30	reserved	-
LADDR+32	Status sysfail register	Master > CPU

Interrupt register CPU > Master

Via this register and the register "Interrupt Register Master > CPU" interrupt requests for the synchronous operating mode (FC 206 - IRQ_RW) are created.

LADDR

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

Possible contents of the register:

- APPLICATION_READY_COMMAND 0Eh

Interrupt register Master > CPU

This register serves the synchronization between CPU and IBS master during the boot sequence. Additionally it serves together with the register "Interrupt Register CPU > Master" for creation of interrupt requests for the synchronous operating mode. After Power-up-Reset and successfully finished self test, the IBS master writes the value C3h into this register.

LADDR+1

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

Possible contents of the register:

- MASTER_READY_COMMAND C3h
- DATA_CYCLE_READY_COMMAND 10h

SSGI acknowledge Master > CPU

LADDR+2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	res.

- Bit 8: Acknowledge-Bit for the message exchange via SSGI (**S**tandard **S**i**g**nal **I**nterface)

SSGI notification Master > CPU

LADDR+4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	res.

- Bit 8: Notification-Bit for the message exchange via SSGI

SSGI result Master > CPU

LADDR+6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	x

- Bit 0: Error during automatic configuration
- Bit 8: Result-Bit for the message exchange via SSGI

SSGI status Master > CPU

LADDR+8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	x

- Bit 0:
  - 0: Automatic start-up is not executed at this time
  - 1: Automatic start-up is executed at this time
- Bit 8: Status-Bit for the message exchange via SSGI

SSGI start CPU > Master

LADDR+10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	x

- Bit 0: Start-Bit for automatic start-up
- Bit 8: Start-Bit for the message exchange via SSGI

Standard funct.-param. register CPU > Master

The register is used by the CPU for transmission of parameters for the standard functions that are activated with the standard function start register.

LADDR+14

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Standard funct. start register CPU > Master

With the help of this registers and the standard functions parameter register you may control the IBS master without using the SSGI. Several often used commands or command sequences may be executed with the two registers. This minimizes the efforts for service requests.

LADDR+16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	res.	res.	res.	res.	res.	res.	res.	x	x	x	x	x	x	x

- Bit 0: Startbit Start_Data_Transfer_Req
  Starts the data transfer.
  – *Precondition:* IBS master is in state ACTIVE
  – *Parameter:* none
- Bit 1: Startbit Alarm_Stop_Req, Activate_Configuration_Req
  Interrupts the data transfer, sets the outputs of all IBS stations to "0" and activates a new configuration frame. Afterwards the IBS master is in state ACTIVE.
  – *Parameter:* Number of the configuration frame to be loaded (e.g. "1")
- Bit 2: Start bit Confirm_Diagnostics_Req
  This bit updates the contents of the diagnosis register and the diagnosis monitors.
- Bit 3: Start bit Control_Active_Configuration_Req Off
  This bit allows you to shut down INTERBUS segments.
  – *Parameter*: The segment-no. has to be stored in the higher valued byte and the position in the lower valued byte. At shut-down of a local bus participant, all stations in the according local bus are shut down. When entering a distant bus station or a bus coupler, besides of the concerning device also the continuative IBS interface is shut down and thus all further IBS stations.
- Bit 4: Start bit Control_Active_Configuration_Req On
  This bit re-activates IBS segments that have been shut down before.
  – *Parameter:* See Bit 3
- Bit 5: Start bit Control_Active_Configuration_Req Disable
  The station set as parameter is toggled in-active within the configuration frame. It may also physically not remain within the data ring and has to be bridged manually.
  – *Parameter:* The segment-no. has to be stored in the higher valued byte and the position in the lower valued byte.
- Bit 6: Start bit Control_Active_Configuration_Req Enable
  The station set as parameter is toggled active again within the configuration frame. It must also physically included back into the data ring.
  – *Parameter:* See Bit 5
- Bit 14: Application-Busy-Bit (at bus synchronous operating mode) res. Data-Cycle-Activate-Bit (at program synchronous operating mode)
- Bit 15: Cons-Activate-Bit for the consistency lock

The bits 14 and 15 serve the processing of protocols for the process data exchange between the IBS master and the CPU.

Standard funct.-status register Master > CPU

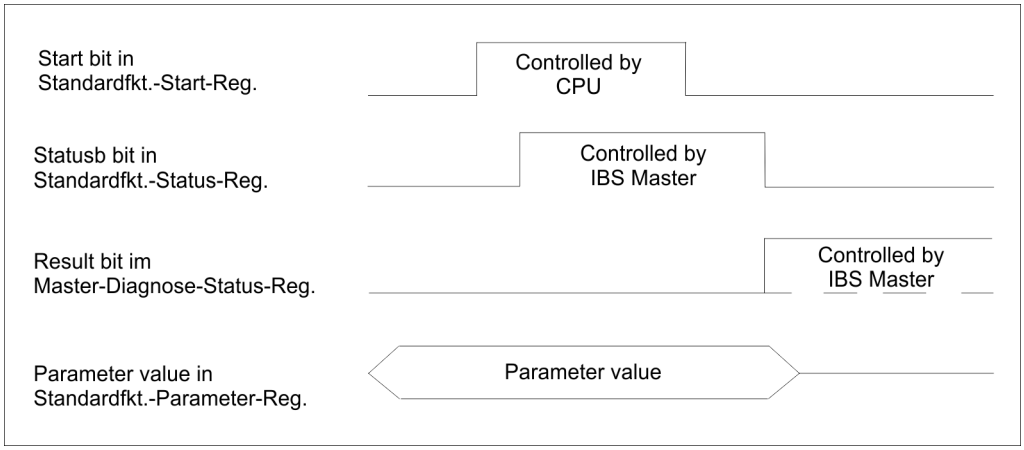
The bits 0...6 of this registers are used by the IBS master to monitor and control the processing of standard functions activated in the standard functions start register. Bit 15 serves the processing of a protocol for the process data exchange between IBS master and the CPU.

LADDR+18

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	res.	res.	res.	res.	res.	res.	res.	res.	x	x	x	x	x	x	x

- Bit 0: Statusbit Start_Data_Transfer_Request
- Bit 1: Statusbit Alarm_Stop_Request, Activate_Configuration_Request
- Bit 2: Statusbit Confirm_Diagnostics_Request
- Bit 3: Statusbit Control_Active_Configuration_Req Off
- Bit 4: Statusbit Control_Active_Configuration_Req On
- Bit 5: Statusbit Control_Active_Configuration_Req Disable
- Bit 6: Statusbit Control_Active_Configuration_Req Enable
- Bit 15: Cons-State-Bit for consistency lock

Execution of a standard function with parameter transfer



⇨ The diagram in the picture above shows the handshake mechanism at usage of the standard functions. A "0" in Bit 10 (RESULT) of the master diagnosis status register shows that the standard function has been finished successful.

Master-Diag.-Param-Register Master > CPU

LADDR+20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

This register monitors depending on the type of the error the error code or the error location. The content of the register is managed by the IBS master. Some error types cause additional entries in the *Extended master diagnosis parameter register*. The contents of the extended master diagnosis parameter register is to be found as word at address 168.0 in the work DB.

Master diag status register Master > CPU

This register contains information about the state of the IBS master. The table contains the meaning of the bits when set ("1"). The content of the registers is managed by the IBS master. In case of an error additional information is available in the master diagnosis parameter register and in the extended master diagnosis parameter register.

LADDR+22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	x	x	res.	res.	x	x	x	x	x	x	x	x	x	x	x

- Bit 0 (USER) User/Parameterization error
- Bit 1 (PF) Periphery failure
- Bit 2 (BUS) Bus failure
- Bit 3 (CTRL) Error at the IBS master
- Bit 4 (DETECT) Diagnosis routine is active
- Bit 5 (RUN) Data transfer is active
- Bit 6 (ACTIVE) Selected INTERBUS configuration ready for operation
- Bit 7 (READY) IBS master ready for operation
- Bit 8 (BSA) Bus segment(s) shut down
- Bit 9 (BASP/SYSFAIL) Function failure of the CPU detected; outputs at the IBS set back
- Bit10 (RESULT) Negative result of a standard function
- Bit13 (WARNING) Defined bus waiting period exceeded
- Bit14 (QUALITY) Defined error density exceeded (is set at more than 20 failures per 1 million IBS cycles)

Slave diag. status register Master > CPU

This register contains information about the state of the optional slave interface to a hierarchical super-ordinated INTERBUS network. The content of the register is managed by the IBS master.

LADDR+26

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	x	x	x	x	x

- Bit 0: COPY
  - 1: Data between IBS master and slave interface are exchanged. The super-ordinated INTERBUS network is operating.
  - 0: No data between IBS master and slave interface are exchanged. The super-ordinated INTERBUS network is not operating.
- Bit 1: FAIL
  - 1: The super-ordinated IBS network has been stopped by a bus error or alarm. No data is exchanged with the slave interface anymore. The output data of the slave interface are set to "0".
  - 0: No error in the super-ordinated INTERBUS network.
- Bit 2: READY-TO-COPY
  - 1: The parameterization of the slave interface has been finished successful.
  - 0: The slave interface has not been parameterized yet.
- Bit 3: POWER-ON
  - 1: The power supply of the slave interface is on.
  - 0: The power supply of the slave interface is off.
- Bit 4: READY
  - 1: The content of the slave diagnosis status register has been initialized.
  - 0: The content of the slave diagnosis status register has been not yet initialized.

Configurations register Master > CPU

In this register it is monitored if the IBS master has finished a parameterization process storage initialized or from operator panel (IBS SWT CMD G4 from Phoenix Contact).

LADDR+28

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	x	res.

- Bit 1: DPM-Node-Par-Ready 1
  - 1: IBS master is parameterized.
  - 0: IBS master is not parameterized.

If a parameterization has been stored in the parameterization memory of the IBS master, the IBS master starts the execution of the stored instructions as soon as it reaches the state READY. Bit 1 is set by the IBS master after all instructions of the parameterization memory has been processed.

Status sysfail register Master > CPU

This register shows a function failure of the CPU that may occur.

LADDR+32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res.	res.	res.	x	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.

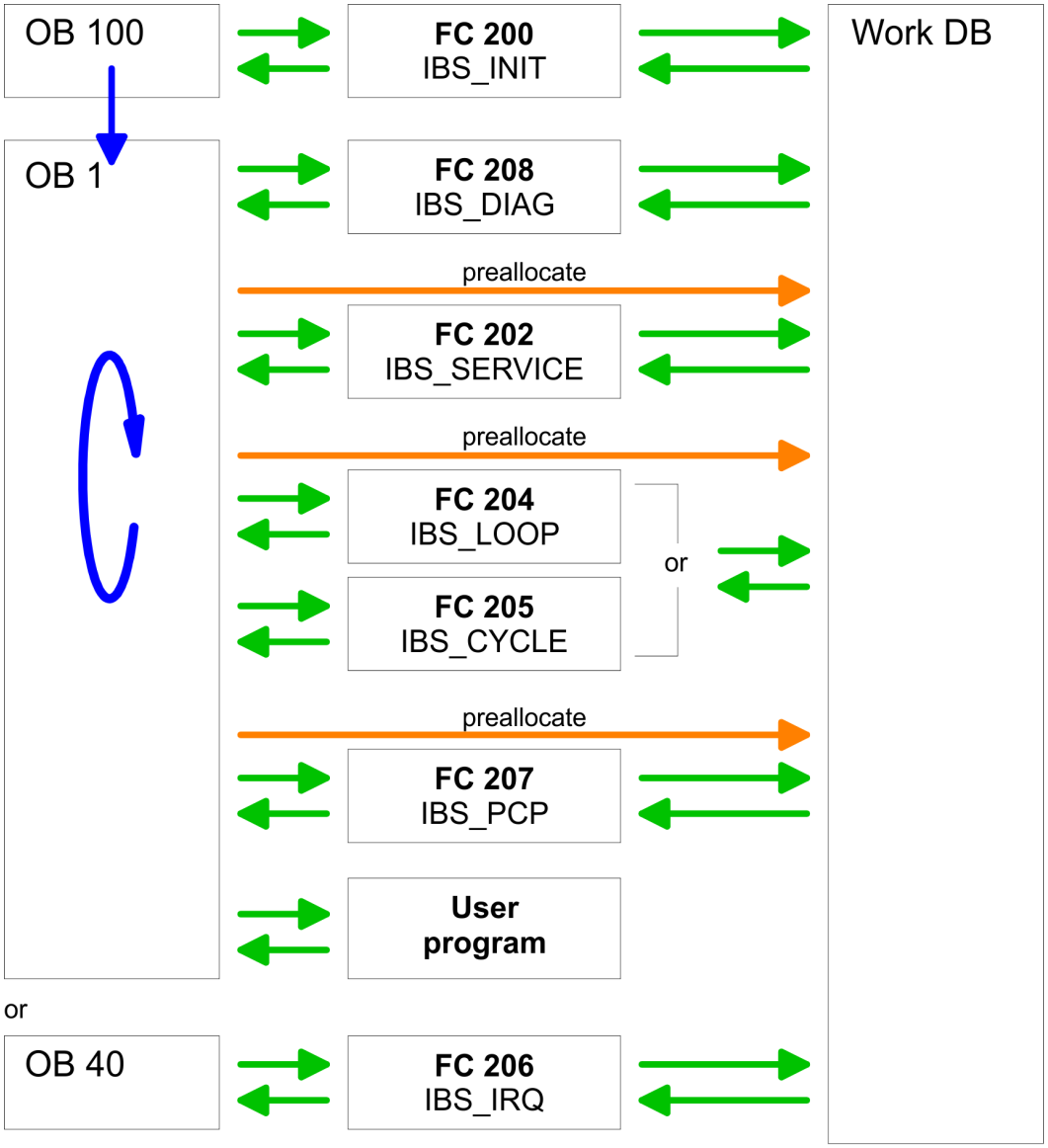
- Bit 12:
  - 1: function failure of the CPU.
  - 0: no function failure of the CPU.

This bit is set by the IBS master when a function failure of the CPU is announced by the interrupt IRQHOSTL. In this case, all outputs of the INTERBUS stations are set to "0". Additionally the diagnosis-LED "HF" is on.

5.6 INTERBUS configuration

Overview

Initialization, diagnosis and data exchange between CPU and IBS master happens via "services" that are transferred by means of VIPA specific handling blocks. The VIPA specific blocks may be found at www.vipa.com as downloadable library at the service area with *Downloads > VIPA LIB*. Please regard for each of the IBS master you have to create a work DB. Each IBS master occupies 34byte in the in-/output address range of the CPU. For the transmission of instructions and parameters to an IBS slave, the "**P**eripherals **C**ommunication **P**rotocol" (PCP) is at your disposal where the transfer also happens with a FC. Your user program should have the following structure:



Before calling the according FCs you have to provide the work DB with parameters!

Please note that SFC 254 RW_SBUS is called internally!

Start address LADDR

To access the IBS1 by means of the handling blocks, for *LADDR* the address preset during hardware configuration is to be used. To access IBS2 you have to add to *LADDR* of IBS1 the value 34. If there is no hardware configuration available, at CPU startup the IBS masters are mapped to the address area of the CPU with the following formulas:

- *Start address IBS1 = 256 (Steckplatz-101)+2048*
- *Start address IBS2 = 256 (Steckplatz-101)+2048 + 34*

5.7 Include FCs

The deployment of the IBS master at the SPEED-Bus happens via the following handling blocks:

Block	Name	Description
FC 200	IBS_INIT	Registration and initialization of an INTERBUS master at the CPU
FC 202	IBS_SERVICE	Service communication between CPU and IBS master
FC 204	IBS_LOOP	Slow asynchronous data communication between CPU and IBS master (waits for master release)
FC 205	IBS_CYCLE	Fast asynchronous data communication between CPU and IBS master (waits not for master release)
FC 206	IBS_IRQ	Synchronous data communication between CPU and IBS master with synchronization via interrupt
FC 207	IBS_PCP	Peripherals Communication Protocol (PCP) communication for instructions and parameters for IBS slaves
FC 208	IBS_DIAG	Read diagnostic data from IBS master res. IBS slaves
SFC 254	RW_SBUS	Communication block, required for usage of the FCs

Installing blocks

The VIPA specific blocks may be found at www.vipa.com as downloadable library at the service area with Downloads > VIPA LIB. The library is available as packed zip-file. If you want to use VIPA specific blocks, you have to import the library into your project. Execute the following steps:

1. Extract Vxxx.zip
2. "Retrieve" the library
3. Open library and transfer blocks into the project

Unzip Vxxx.zip

Start your un-zip application with a double click on the file Vxxx.zip and copy the file vipa.zip to your work directory. It is not necessary to extract this file, too.

Retrieve library

To retrieve your library for the SPEED7-CPUs, start the SIMATIC manager from Siemens. Open the dialog window for archive selection via **File** > *Retrieve*. Navigate to your work directory. Choose VIPA.ZIP and click at [Open]. Select a destination folder where the blocks are to be stored. [OK] starts the extraction.

Open library and transfer blocks to project

After the extraction open the library. Open your project and copy the necessary blocks from the library into the directory "blocks" of your project. Now you have access to the VIPA specific blocks via your user application.

Structure of the "Work DB"

You have to create a work DB for each IBS master. You may download this DB together with a sample project at www.vipa.com at the service area. The following table shows the structure of the work DB. Parameters that must be set before calling the according FC are highlighted.

Include FCs

Addr.	Name	Type	Comment
0.0	free	BYTE	
1.0	free_1	BYTE	
2.0	Addr_INT_Host_Mas	DWORD	Address of the interrupt Host-->Master 0xFFF
6.0	Addr_INT_Mas_Host	DWORD	Address of the interrupt Master-->Host 0xFFE
10.0	Addr_SSGI_Ack	DWORD	Address SSGI acknowledge 0xFDE
14.0	Addr_SSGI_Notif	DWORD	Address SSGI notification 0xFE0
18.0	Addr_SSGI_Result	DWORD	Address SSGI result 0xFE2
22.0	Addr_SSGI_Status	DWORD	Address SSGI status 0xFE4
26.0	Addr_SSGI_Start	DWORD	Address SSGI start 0xFE6
30.0	reserved	DWORD	
34.0	Addr_Stand_Fct_Param	DWORD	Address standard function parameter 0xFEA
38.0	Addr_Stand_Fct_Start	DWORD	Address standard function start 0xFEC
42.0	Addr_Stand_Fct_Status	DWORD	Address standard function status 0xFEE
46.0	Addr_Master_Diag_Param	DWORD	Address Master diagnosis parameter 0xFF0
50.0	Addr_Master_Diag_Status	DWORD	Address Master diagnosis status 0xFF2
54.0	reserved_2	DWORD	
58.0	Addr_Slave_Diag_Status	DWORD	Address Slave diagnosis status 0xFF6
62.0	Addr_Configuration	DWORD	Address Configuration 0xFF8
66.0	reserved_3	DWORD	
70.0	Addr_Status_Sysfail	DWORD	Address status system error 0xFFC
74.0	SSGI_Ack	WORD	Register value SSGI Acknowledge
76.0	SSGI_Notif	WORD	Register value SSGI Notification
78.0	SSGI_Result	WORD	Register value SSGI result
80.0	SSGI_Status	WORD	Register value SSGI status
82.0	SSGI_Start	WORD	Register value SSGI start
84.0	reserved_4	WORD	
86.0	Stand_Fct_Param	WORD	Register value standard function parameter
88.0	Stand_Fct_Start	WORD	Register value standard function start
90.0	Stand_Fct_Status	WORD	Register value standard function status
92.0	Master_Diag_Param	WORD	Register value Master diagnosis parameter
94.0	Master_Diag_Status	WORD	Register value Master diagnosis status
96.0	reserved_5	WORD	
98.0	Slave_Diag_Status	WORD	Register value Slave diagnosis status
100.0	Configuration	WORD	Register value Configuration
102.0	reserved_6	WORD	
104.0	Status_Sysfail	WORD	Register value status system error

Addr.	Name	Type	Comment
106.0	Step_Counter_Service	INT	Step counter for FC 202 "process services"
108.0	RET_VALSEND_Service	WORD	Return value of the SFC 254 at send command via FC 202
110.0	RET_VALRECEIVE_Service	WORD	Return value of the SFC 254 at read command via FC 202
112.0	Error_Byte_Service	BYTE	Error ID of FC 202
113.0	Number_Service_Error	BYTE	Number of the service where the error has been detected.
114.0	Return1_Function_Service	WORD	Error code 1 return value of the service
116.0	Return2_Function_Service	WORD	Error code 2 return value of the service
118.0	**Number_Services**	**BYTE**	**Number of services to process for FC 202**
119.0	Processed_Services	BYTE	Number of processed services
120.0	Waiting_Receipt	WORD	Interim storage of expected acknowledgement
122.0	Start_Services	BYTE	Number of service that is 1. to process
124.0	Waiting_Time	S5TIME	Waiting period for acknowledgements
126.0	Timer_No	WORD	Timer number for waiting period
128.0	Extended_Diagnosis	BYTE	Bit 0 bit memory bit when extended diagnosis requested
129.0	Additional03	BYTE	
130.0	**DB_No_Write**	**WORD**	**DB_No. of output data (for FC 204/FC 205 if data in DB)**
132.0	**Start_Data_In**	**WORD**	**Address of 1. output byte (for FC 204/205)**
134.0	**Length_Data_In**	**WORD**	**Length of output data (for FC 204/205)**
136.0	**Start_Data_DPM_In**	**WORD**	Start address of output data in DPM (for FC 204/205)
138.0	**DB_No_Read**	**WORD**	**DB-No. of input data (for FC 204/205 if data in DB)**
140.0	**Start_Data_Out**	**WORD**	**Address of 1. input byte (for FC 204/205)**
142.0	**Length_Data_Out**	**WORD**	**Length of input data (for FC 204/205)**
144.0	**Start_Data_DPM_Out**	**WORD**	**Start address of input data in DPM (for FC 204/205)**
146.0	RET_VAL_DATEN_SEND	WORD	Return value of the SFC 254 at writing data via FC 204/205
148.0	RET_VAL_DATEN_REC	WORD	Return value of the SFC 254 at reading data via FC 204/205
150.0	Error_Data_L_S	WORD	Error byte of the FC 204/FC205
152.0	Step_FC205	BYTE	Read/Write step counter I/O of FC 205
153.0	Additional013	BYTE	
154.0	Step_FC208	WORD	Step counter of FC 208
156.0	Order_Diag_316	WORD	Enter command for transmission (316 fix)
158.0	Parameter_Order_316	WORD	Number of parameters for command (316 fix)
160.0	Error_Service_FC208	BYTE	Error byte of the FC 208
161.0	Control_bit_FC208	BYTE	Control bits of the FC 208
162.0	Waiting_period_Auto	S5TIME	Waiting period at auto start after error
164.0	RET_VAL_SFC_FC208	WORD	Return value of the SFC 254 at read/write data via FC 208
166.0	Timer_FC208	WORD	Number additional timer (Number = Timer_No +1)

Include FCs

Addr.	Name	Type	Comment
168.0	Extension_Diagnosis_Param	WORD	Diagnostic addition to master diagnosis parameter register
170.0	Number_Bus_Errors	INT	Error counter of all bus disruptions
172.0	Number_IBSUSC4_Errors	INT	Error counter of all IBS USC4 errors
174.0	Number_Peripherie_Errors	INT	Error counter of all periphery errors
176.0	Number_User_Errors	INT	Error counter of all user errors
178.0	Order_Diag_315	WORD	Enter command for transmission (315 fix)
180.0	Parameter1_Order_315	WORD	Number of parameters for command (315 fix)
182.0	Parameter2_Order_315	WORD	Parameters for command 315
184.0	Waiting_Period_Detection	S5TIME	Waiting period for detection
186.0	Step_Counter_PCP	INT	Step counter of FC 207
188.0	RET_VALSEND_PCP	WORD	Return value of the SFC 254 at send command via FC 207
190.0	RET_VALRECEIVE_PCP	WORD	Return value of the SFC 254 at read command via FC 207
192.0	Error_Byte_PCP	BYTE	Error byte of the FC 207
193.0	Number_PCP_Errors	BYTE	Number of the PCP where error has been detected
194.0	DW_Counter_PCP	DWORD	Number of error codes returned from the PCP
198.0	**Number_PCP**	**BYTE**	**Number of PCP to be processed for FC 207**
199.0	Processed_PCP	BYTE	Number of already processed PCP
200.0	Waiting_Receipt_PCP	WORD	ID of expected acknowledgement
202.0	Start_PCP	BYTE	Number of 1. PCP to be processed
204.0	Error1_PCP	WORD	Error code 1 Return value of the PCP
...	...	...	...
218.0	Error8_PCP	WORD	Error code 8 Return value of the PCP
220.0	Adress_SFC254	WORD	Module address for SFC 254
222.0	Additional110	BYTE	
...	...	...	...
249.0	Additional137	BYTE	
250.0	Diagnosis_Bus_Error[1]	BYTE	Entry of extended diagnosis at bus error
...	...	...	...
299.0	Diagnosis_Bus_Error[50]	BYTE	
300.0	Diagnosis_IBSUBC4_Error[1]	BYTE	Entry of extended diagnosis at IBS UBC4 error
...	...	...	...
349.0	Diagnosis_IBSUBC4_Error[50]	BYTE	
350.0	Diagnosis_Periph_Error[1]	BYTE	Entry of extended diagnosis at periphery error
...	...	...	...
399.0	Diagnosis_Periph_Error[50]	BYTE	
400.0	Diagnosis_USER_Error[1]	BYTE	Entry of extended diagnosis at user error

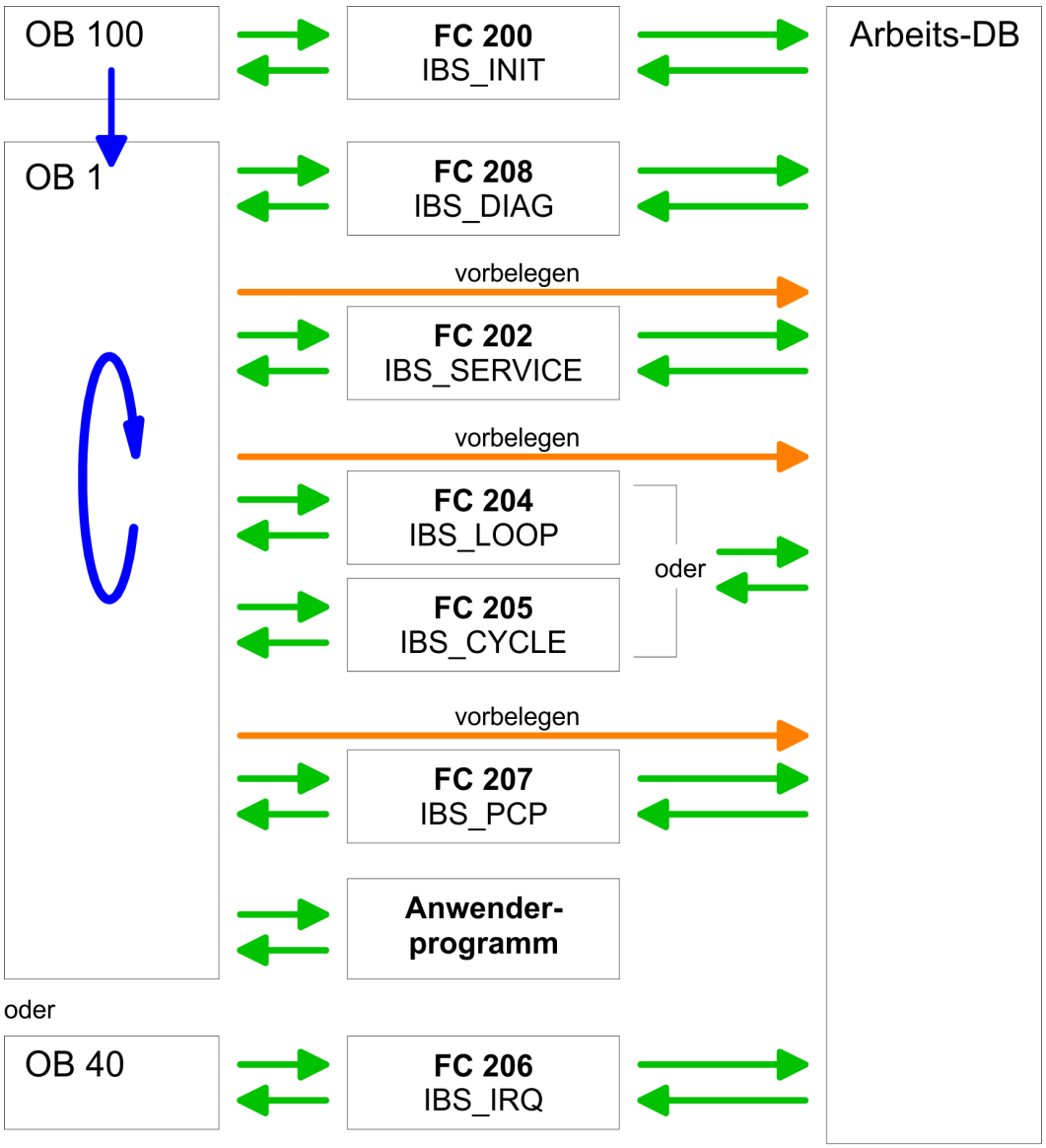
Addr.	Name	Type	Comment
...	...	...	...
449.0	Diagnosis_USER_Error[50]	BYTE	

Program structure

The INTERBUS functions have to be called at boot of the CPU and in the cyclic program by means of conditional or absolute jumps. You have to include the FC 200 in the boot sequence. This FC synchronizes the IBS master with the CPU and checks the structure of the connected in- and output bytes as well as the bus structure. Via the FC 208 you may read diagnostic data of the master res. the slaves in the cyclic program. This block also sets the starting type of the IBS master after an error. You may parameterize the IBS master via the FC 202. For this you have to transmit a DB that may contain up to 30 service instructions. Before this you must enter the number of services in the work DB under "Number_services". By calling FC 204 or FC 205 the asynchronous data exchange between IBS master and the CPU starts. Both FCs have the same request parameters. The FC 204 waits after the data request for the data release of the IBS master and then continues the cycle process. In opposite to FC 204, the FC 205 does not wait. As long as no data release is present, it continues the cycle processing. Thus the cycle processing of the CPU is not interrupted. You may also synchronize the data transfer by using the FC 206 instead and call this within a HW-Interrupt-OB. Here the IBS master announces new data via an interrupt. Reading of data by the CPU is also signalized via an interrupt.

User application

Your user application should have the following structure:



5.7.1 Function blocks

In the following you will find a more detailed description of the function blocks that are required for the Interbus communication.

5.7.1.1 FC 200 - IBS_INIT

Description

This FC synchronizes the INTERBUS master with the CPU and checks the number of connected in- and output bytes as well as the bus structure.

Parameters

Parameter	Declaration	Data type	Description
WORK_DB	IN	BLOCK_DB	INTERBUS work DB
LADDR	IN	INT	Logical base address of INTERBUS master
MODE	IN	INT	Mode for start-up
WAIT_TIME	IN	S5TIME	Wait time for INTERBUS Master acknowledgement
TIMER_NO	IN	INT	Timer number for wait time
SERVICE_DB_SEND	IN	INT	DB number with services
SERVICE_DB_REC	IN	INT	DB number for INTERBUS master acknowledgement
NO_OF_SERVICES	IN	Word	Number of services to be processed starting at FIRST_SERVICE
READ_DIAG	IN	BOOL	Structure diagnostic data
RET_VAL	OUT	WORD	Return value on error
FIRST_SERVICE	IN_OUT	BYTE	Number of 1. service of the service DB to be processed

WORK_DB

Set the work DB for the wanted master.

LADDR

Set the address (**L**ogical **Addr**ess) from where on the register of the masters is to be mapped into the CPU. At start-up of the CPU, the INTERBUS master are mapped into the I/O address range of the CPU with the following formula if no hardware configuration is present:

Start address = 256× (Slot-101)+2048

The slot numbering at the SPEED-Bus starts with 101 at the left side of the CPU and ascends from the right to the left.

For example, the 1. slot has the address 2048, the 2. the address 2304 etc...

MODE

This parameter allows you to preset the following modes for start-up:

0 = Calculate address only

1 = Calculate address and wait for Ready of the INTERBUS master

2 = Calculate address, parameterize and start INTERBUS master

3 = Calculate address and automatically start of INTERBUS after auto-configuration via switch

WAIT_TIME TIMER_NO

Here you may define a waiting period with the according timer by setting *WAIT_TIME* and *TIMER-NO* that the CPU has to wait for a master acknowledgment after a service command.

Please regard at setting a timer number. That always 2 sequential timers are used:

Timer 1: TIMER_NO, Timer 2: TIMER_NO + 1

SERVICE_DB_SEND, SERVICE_DB_REC

Enter the DB that contains the according service instructions via *SERVICE_DB_SEND*. In *SERVICE_DB_REC* the INTERBUS master returns the receipt. ↬ *'Structure service DB ' on page 51*

NO_OF_SERVICES, FIRST_SERVICE

In *NO_OF_SERVICES* you enter the number of services that have to be processed in the service DB after the 1. service that you set in *FIRST_SERVICE.*

READ_DIAG

This parameter allows you to influence the structure of a diagnosis:

0 = Normal diagnosis

1 = Extended diagnosis

RET_VAL

In case of an error, *RET_VAL* may contain the following error messages:

1 = Waiting period for master receipt (READY) exceeded - master not ready

2 = Execution of a service to process has failed

5.7.1.2 FC 202 - IBS_SERVICE

Description

This function block allows you to transfer services to the INTERBUS master and to react to the according acknowledgements.

For the INTERBUS master card USC4-1 from Phoenix Contact is deployed as INTERBUS hardware platform, please also refer to the extensive documentation (IBS SYS FW G4 UM) from Phoenix Contact for the description of the INTERBUS services and INTERBUS error messages.

Parameters

Parameter	Declaration	Data type	Description
WORK_DB	IN	BLOCK_DB	INTERBUS work DB
SERVICE_DB_SEND	IN	INT	DB number with services
SERVICE_DB_REC	IN	INT	DB number for INTERBUS master acknowledgement
FIRST_SERVICE	IN	BYTE	Number of 1. service of the service DB to be processed
START	IN_OUT	BOOL	Start bit of the function
ERROR	IN_OUT	BOOL	Error bit of the function

WORK_DB

Set the work DB for the wanted master.

SERVICE_DB_SEND, SERVICE_DB_REC

Enter the DB that contains the according service instructions via *SERVICE_DB_SEND*. In *SERVICE_DB_REC* the INTERBUS master returns the receipt.

FIRST_SERVICE

Enter the position of the first service within the send DB.

Please regard that you have to enter the number of services that are to be transferred after FIRST_SERVICE in the work DB before calling the FC 202.

Structure service DB

You may enter a max. of 30 services in one DB. Up to 2 DBs, 60 services in total, may be transferred to the INTERBUS master at every FC call.

DBB	Contents
0 ... 69	Record set 1
70 ... 139	Record set 2
...	. . .
2030 ... 2099	Record set
2100	Instruction number 2. DB

Structure record set

DBW	Contents
0	Send length (Number of bytes to be send)
1	Code number of service
2	Parameter count
3 ... 68	Parameter

START

By setting the start bit, the services are transferred to the INTERBUS master and started.

ERROR

In case of an error, the Start bit is set back and the error bit is set. Additionally, the number of the service that has been processed when the error occurred is entered in the DBB113 of the work DB. The error code is displayed in DBB112.

The following error codes may occur:

2 = Error of the master at reading data from SSGI Box

3 = Return code of the acknowledgement not valid

4 = Service could not be processed

5 = No acknowledgement within waiting period

If DBB112 contains the error code 4, further error codes are entered into DBW114 and 116 of the work DB. Information about these error codes is to be found in the documentation of the services (IBS SYS FW G4 UM) from Phoenix Contact.

5.7.1.3 FC 204 - IBS_LOOP, FC 205 - IBS_CYCLE

Description

The FC 204 serves the exchange of in- and output data between INTERBUS master and CPU. This block always awaits an acknowledgement of the master after a data request and continues the cycle processing only after reception.

If this block influences the cycle processing of the CPU too much, you should use the FC 205 Asynchr_Cycle instead. In opposite to the FC 204 this does not wait for an acknowledgement but continues cycle processing after data request.

Occurring error messages are to be found after block processing in the work DB in DBW150.

Parameters

Parameter	Declaration	Data type	Description
WORK_DB	IN	BLOCK_DB	INTERBUS work DB
RW_MODE	IN	INT	Mode of Read/Write (0=R/W, 1=R, 2=W)
OPERATION_MODE	IN	INT	Operation mode (0=asynchr., 1=asynchr. with consistency)
TYP_OUT	IN	INT	Data type of INTERBUS slave out data (0=DB, 1=MB, 2=OB)
TYP_IN	IN	INT	Data type of INTERBUS slave in data (0=DB, 1=MB, 2=IB)
START	IN_OUT	BOOL	Start bit of the function

WORK_DB

Set the work DB for the wanted master.

RW_MODE

The following modes are available:

0 = Read input data and write output data

1 = Read input data only

2 = Write output data only

OPERATION_MODE

The transfer may happen with the following operating modes:

0 = Asynchronous data exchange without consistency lock

In this operating mode it may happen that read res. written data is not out of the same INTERBUS cycle and is therefore inconsistent.

1 = Asynchronous data exchange with consistency lock

Here the CPU sets a bit for read/write request. As soon as the next INTERBUS cycle is finished and data is ready, the INTERBUS master sets a release bit. The CPU transfers its data and signalizes the end of data transfer by setting back the request. Now the INTERBUS master deletes the release and continues the INTERBUS cycle.

TYP_OUT, TYP_IN

This parameter defines the type of the data area where the I/O data of connected INTERBUS slaves is stored.

The following types are available:

0 = DB (data block)

1 = MB (bit memory byte)

2 = I/O range of the CPU

START

By setting the Start bit, the FC is executed. The start is set back again in the block.

Error message

During the execution of the block, the following errors that are stored in DBW 150 of the work DB may occur:

1 = Data release of the master missing - read inputs

2 = Data release of the master missing - write outputs

3 = Data release of the masters is not deleted

5.7.1.4 FC 206 - IBS_IRQ

Description

At deployment of the FC 206, the data transfer of the in- and output data between CPU and INTERBUS master is controlled via interrupts.

As soon as the INTERBUS master has provided its data, it initializes an interrupt. The CPU transfers its data and also signalizes the end of the data transfer via an interrupt. Now the INTERBUS master continues the INTERBUS cycle.

Parameters

Parameter	Declaration	Data type	Description
WORK_DB	IN	BLOCK_DB	INTERBUS work DB
RW_MODE	IN	INT	Mode of R/W (0=R/W, 1=R, 2=W)
TYP_OUT	IN	INT	Data type of INTERBUS slave out data (0=DB, 1=MB, 2=OB)
TYP_IN	IN	INT	Data type of INTERBUS slave in data (0=DB, 1=MB, 2=IB)

WORK_DB

Set the work DB for the wanted master.

RW_MODE

The following modes are available:

0 = Read input data and write output data

1 = Read input data only

2 = Write output data only

TYP_OUT, TYP_IN

This parameter defines the type of the data area where the I/O data of connected INTERBUS slaves is stored.

The following types are available:

0 = DB (data block)

1 = MB (bit memory byte)

2 = I/O range of the CPU

5.7.1.5 FC 207 - IBS_PCP

Description

This function block allows you to transfer PCP services to the INTERBUS master and to react to the according acknowledgements. The **P**eripherals **C**ommunication **P**rotocol (PCP) serves the transmission of instructions and parameters to connected slaves and the reception of acknowledgements and data of the slaves.

Information about the services is to be found in the documentation of the services, available via our application department.

Parameters

Parameter	Declaration	Data type	Description
WORK_DB	IN	BLOCK_DB	INTERBUS work DB
SERVICE_DB_SEND	IN	INT	DB number with services
SERVICE_DB_REC	IN	INT	DB number for INTERBUS master acknowledgement
FIRST_SERVICE	IN	Byte	Number of 1. service of the service DB to be processed
START	IN_OUT	BOOL	Start bit of the function
ERROR	IN_OUT	BOOL	Error bit of the function

WORK_DB

Set the work DB for the wanted master.

SERVICE_DB_SEND, SERVICE_DB_REC

Enter the DB that contains the according PCP service instructions via *SERVICE_DB_SEND*. In *SERVICE_DB_REC* the slaves return the receipt.

FIRST_SERVICE

Enter the position of the first PCP service within the send.

Please regard that you have to enter the number of services that are to be transferred after FIRST_SERVICE in the work DB before calling the FC 207.

Structure service DB

You may enter a max. of 30 PCP services in one DB. Up to 2 DBs, 60 PCP services in total, may be transferred to the INTERBUS master at every FC call.

DBB	Content
0 ... 69	Record set 1
70 ... 139	Record set 2
...	...
2030 ... 2099	Record set 30
2100	Sequence number of 2. DB

Structure record set

DBW	Content
0	Send length (Number of bytes to be send)
1	Code number of PCP service
2	Parameter count
3 ... 68	Parameter

START

By setting the start bit, the PCP services are transferred to the INTERBUS master and started.

ERROR

In case of an error, the start bit is set back and the error bit is set. Additionally, the number of the PCP service that has been processed when the error occurred is entered in the DBB193.

The following error codes may be entered into DBB192:

2 = Error of the master at reading data from SSGI Box

3 = Return code of the acknowledgement not valid

4 = Service could not be processed

5 = No acknowledgement within waiting period

If ERROR contains the error code 4, further error codes are entered into DBW194 and 196 of the work DB. Information about these error codes is to be found in the documentation of the error codes, available via our application department.

5.7.1.6 FC 208 - IBS_DIAG

Description

Via this function block you may read diagnostic data from the master res. slave in case of an INTERBUS breakdown. Here you may also define the reboot operating mode of the INTERBUS master after breakdown.

Parameters

Parameter	Declaration	Data type	Description
WORK_DB	IN	BLOCK_DB	INTERBUS work DB
ACTIVATE	IN	INT	Manual error acknowledgement
AUTO_START	IN	INT	Automatic error acknowledgement
RUN	OUT	Byte	Status INTERBUS in RUN
PERIPHERAL_ERROR	OUT	BOOL	Error at periphery
BUS_QUALITY	OUT	BOOL	Sporadic bus errors occurred
DETECTION	OUT	BOOL	Internal error is searched
BUSY_STATE	OUT	BOOL	Internal diagnostic function is busy

WORK_DB Set the work DB for the wanted master.

ACTIVATE, AUTO_START The *ACTIVATE* transmission parameter of the type Boolean that you may control for example via an external caliper, allows you to reboot the INTERBUS master by setting (push button).

By setting of auto-start, the INTERBUS master reboots automatically after error recovering. *AUTO-START* has always preference before *ACTIVATE*.

RUN This parameter shows the status of the INTERBUS master:

0 = INTERBUS master is in STOP

1 = INTERBUS master is in RUN

PERIPHERAL_ ERROR If a periphery error occurs, the INTERBUS master announces PF = 1. At PF = 0 no periphery error occurred.

In case of an error you will see the number of the causing slave in the work DB starting with 1.

BUS_QUALITY This parameter displays information about the transfer quality within the INTERBUS. As soon as the bit is set by the INTERBUS master, some single transmission interferences have occurred. Please check the transfer routes with according diagnosis software.

DETECTION The parameter *DETECTION* is set by the INTERBUS master when the internal error detection is running. When the error detection is finished, *DETECTION* is set back again.

BUSY_STATE When a diagnosis is executed within the diagnosis block, *BUSY_STATE* is set. As soon as diagnosis data are available, the block sets *BUSY_STATE* back again.

5.8 Diagnostics

General

For diagnostics of the operating and fault conditions each INTERBUS master has a RJ45 jack to connect the VIPA diagnostics device 342-0IA01. The device has a multi line LCD display for display and a key field for menu-assisted service. The hardware platform of the diagnostics device (USC/4-DIAG-L) comes from Phoenix Contact as like the IBS hardware platform of the master (USC4-2). In the following the single components are described only briefly. In the "Diagnostics guide" of Phoenix Contact a detailed description of the diagnostics possibilities may be found.

Connect the diagnostics device

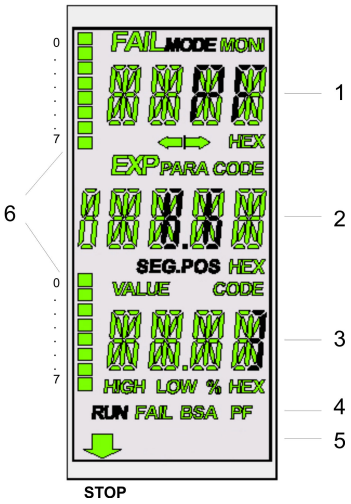
The diagnostics device is directly supplied by the RJ45 jack of the IBS master and is ready for use after connection.

CAUTION!
Please consider the sufficient grounding when connecting the diagnostics device. Hardware-caused there is the risk to come in contact to a pin of the plug while the diagnostics device is connected. This could damage the device by an electrostatic discharge.

LCD Display

The diagnostic display consists of the following components:

- 3 main lines to display operating states, addresses and data.
- 16 status segments on the left side of the display for binary representation of input and output data.
- CPU STOP status indicator (Arrow is displayed).
- Red (error) or green (normal operation) background illumination, depending on the operating state of the bus

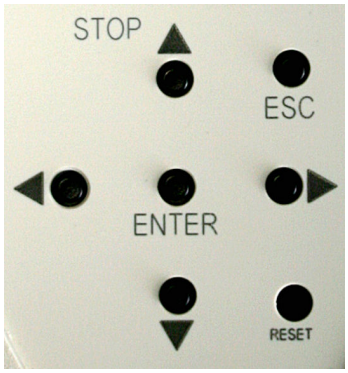


[1]	**FAIL**	Indicates that an error has occurred and provides information about the error type.	
		CTRL	Controller error
		RBUS	Remote bus error
		LBUS	Local bus error
		BUS	General bus error
		OUT1	Error at the outgoing interface
		OUT2	Error at the branching interface
		DEV	Device error
		PF	Peripheral fault
	MODE	When MODE active, further menu items may be selected.	
	MONI	Indicates that monitor mode is activated.	
	HEX	The value in the 1. main line is displayed in hexadecimal notation. If the HEX segment is not activated, the value is displayed in decimal notation.	
[2]	**PARA**	The displayed value is a parameter of a message.	
	CODE	The displayed value represents a code.	
	SEG.POS	The displayed value is a device number (bus segment and position).	
	HEX	The value in the 2. main line is displayed in hexadecimal notation. If the HEX segment is not activated, the value is displayed in decimal notation.	
[3]	**VALUE**	The displayed number is a value.	
	CODE	The displayed value represents a code.	
	HIGH	The displayed number is a high-order word of a 32bit value.	
	LOW	The displayed number is a low-order word of a 32bit value.	
	%	The displayed number is a percentage term.	
	HEX	The value in the 3. main line is displayed in hexadecimal notation. If the HEX segment is not activated, the value is displayed in decimal notation.	
[4]	**RUN**	Indicates the current operating state of the IBS master: ■ Off: INTERBUS at state READY or BOOT ■ Flashes: INTERBUS at state ACTIVE ■ On: INTERBUS at state RUN	
	FAIL	Active in the event of controller, user or bus errors.	
	BSA	(**B**us **S**egment **A**borted) Active when a bus segment is switched off and inactive when all segments are switched on again.	
	PF	(**P**eripheral **F**ault) Active when a device indicates a peripheral fault.	

[5]	**CPU-STOP-status**	If the superimposed CPU is in STOP state, an arrow appears in the bottom line of the display pointing to the "STOP" label of the front panel.
[6]	**Statussegments**	The 16 status segments for the binary representation of in and output words, are indicated, if an appropriate menu were opened.

Keypad

The keypad enables menu-driven operation of the diagnostics display using the arrow keys.



Key	Description
▲	Go up
▼	Go down
▶	Selection of a menu item or address
◀	Selection of a menu item or address
ENTER	Confirm selection
ESC	Exit menu item or switch to the next level up
RESET	This button is reserved for internal functions and is deactivated at diagnostics operation

Selecting a menu item

Different menu items may be selected on the display. You can move within a menu level using the ◀ ▶. To jump to the next level down, confirm the selected menu item by pressing ENTER. The currently selected menu item is always shown in the 1. line. If there is another level under this menu item, the name of one of the available menu items will flash in the 2. line. Press ESC to return to the previous level.

Menu structure

To access the MODE and MONI menu items from the standard view, press ▶

MODE	Here you may get information about the current bus configuration and status. Statistical data about the state of the bus system can also be requested e.g., the error frequency of specific devices. Further general information such as the firmware version or the serial number are centralized.
MONI	Via the MONI item the states of inputs and outputs may be displayed. This monitor function is adapted to the addressing syntax of the CPU.

5.9 Firmware update

Overview

There is the possibility to execute a firmware update of the CP 342-2IA71 among others via the SPPED7 CPU by means of a memory card. So a firmware file may be recognized and assigned with startup, a pkg file name is reserved for each updateable component and hardware release. This file name begins with "px" and differs in a number with six digits. The pkg file name may be found at a label right down the front flap of the module.

Latest firmware at www.vipa.com

The latest firmware versions may be found in the service area at www.vipa.com.

For example the following file is necessary for the firmware update of the CP 342-2IA71 with hardware release 01:

Px000109.pkg

CAUTION!
When installing a new firmware you have to be extremely careful. Under certain circumstances you may destroy the CP, for example if the voltage supply is interrupted during transfer or if the firmware file is defective. In this case, please call the VIPA-Hotline! Please regard that the version of the update firmware has to be different from the existing firmware otherwise no update is executed.

Display the Firmware version of the SPEED7 system via Web Site

The CPU has an integrated website that monitors information about firmware version of the SPEED7 components. The Ethernet PG/OP channel provides the access to this web site. To activate the PG/OP channel you have to enter according IP parameters. This can be made in Siemens SIMATIC manager either by a hardware configuration, loaded by MMC respectively MPI or via Ethernet by means of the MAC address with **PLC** > *Assign Ethernet Address*. After that you may access the PG/OP channel with a web browser via the IP address of the project engineering. More detailed information may be found in the CPU manual at "Access to Ethernet PG/OP channel and website".

Load firmware and transfer it to MMC

1. Go to www.vipa.com
2. Click on Service > Download > Firmware Updates.
3. Click on "Firmware for System 300S"
4. Choose the according CP modules and download the firmware Px.....zip to your PC.
5. Extract the zip-file and copy the extracted file to your MMC. Following this approach, transfer all wanted firmware files to your MMC.

CAUTION!
With a firmware update an overall reset is automatically executed. If your program is only available in the load memory of the CPU it is deleted! Save your program before executing a firmware update!

Transfer firmware from MMC to the CP

1. Get the RUN-STOP lever of your CPU in position STOP. Turn off the voltage supply. Plug the MMC with the firmware files into the CPU. Please take care of the correct plug-in direction of the MMC. Turn on the voltage supply.
2. After a short boot-up time, the alternate blinking of the CPU-LEDs SF and FRCE shows that at least a more current firmware file was found on the MMC.

3. 3. You start the transfer of the firmware to the CP as soon as you tip the RUN/STOP lever downwards to MRES within 10s. Now every CP 342-2IA71 at the SPEED-Bus gets a firmware update.
4. During the update process at the CPU the LEDs SF and FRCE are alternately blinking and the MCC LED is on. Please regard the update procedure is exclusively indicated by the LEDs of the CPU.
5. The update is successful finished when the LEDs PWR, STOP, SF, FRCE and MCC of the CPU get on. If they are blinking fast, an error has occurred.
6. Turn Power OFF and ON. Now your CP is ready for operation.

More about firmware update may be found in the manual of the SPEED7 CPU at chapter "Deployment CPU ..." at "Firmware update".

5.10 Example

Overview

The following sample shall illustrate a communication between a SPEED-Bus-IBS master and a connected IBS slave. The example is to be found in the service area at www.vipa.com as "300S-Demo-Interbus.zip". After the download you may load the .zip file as project into the SIMATIC Manager from Siemens via **File** > *De-archivate*.

Properties

The sample project provides the following features:

- Appropriate for deployment at a VIPA IBS master CP.
- The addressing of the IBS master happens automatically (no hardware configuration). The IBS master must be at the 1. slot at the SPEED-Bus for it works with module address 2048. Otherwise you have to adjust the *LADDR* parameter for the FC 202 accordingly.
- For the IBS configuration is newly detected at reboot, the number of connected IBS slaves is irrelevant.
- During the hardware configuration the Ethernet PG/OP channel is assigned to the IP address 172.16.129.71. With this IP address you may access the CPU online via the Ethernet PG/OP channel. Please consider to adjust the IP address accordingly if you are working with another number circle.

Program structure

For the program has comment at according lines, here you will only find the basic structure.

OB 100 Boot/Reboot

- Presetting of services for automatic start.
  - Service 1303h Stop bus
  - Service 0710h Read configuration automatically
  - Service 0701h Start bus communication (master → slave)
- Call function for initialization of the master
- Set control bit for cyclical reading
- Set control bit for automatic start after error

OB 1

- Call FC 1000

OB 40

- Call sample at interrupt controlled data transfer

FC 1000 master processing

- Read diagnosis
- Detect status IBS master (RUN/STOP)
- Call the function for service processing
- Preset data in work DB (DB 120) for read and write accesses of the IBS I/Os
- Read and write IBS I/Os
- Initialize again read and write

DB 10, UDT1, DB 11

- For every service, an entry of the type „service“ is to be found in *DB 10*. The data type of "service" is defined under *UDT1*.

DB 11

- Acknowledgement DB is the DB 11..

DB 110

- If you want to transfer more than 30 services, you may set a pointer to another service DB in DB 10 (here DB 110). This is monitored in OB 100.

SFC 254

- The SFC 254 is required for the communication between CPU and IBS master. The call of the SFC 254 happens from IBS-FCs (FC 200 ... FC 208).

SFC 1

- The system block SFC 1 is automatically created when you call the FC 208 "Diagnostic".