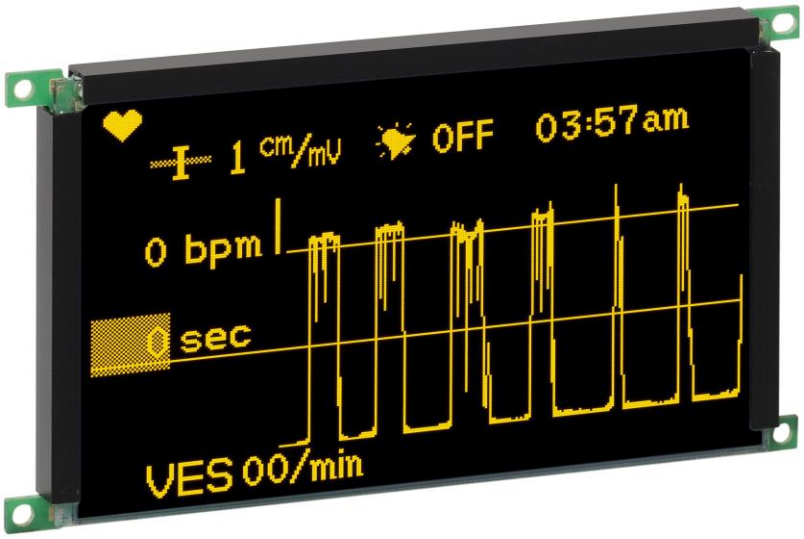

EL240.128.45

Operation Manual

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1 EL240.128.45 display

The EL240.128.45 thin film electroluminescent (TFEL) small graphics display utilizes Lumineq® Displays' proprietary Integral Contrast Enhancement (ICEBrite™) technology to achieve unparalleled image quality without the use of expensive filters. This small graphics display excels in a wide range of ambient lighting environments while effectively eliminating the blooming common to other high-bright displays.

The display consists of a TFEL glass panel and control electronics connected using elastomeric interconnects into a space-saving, rugged package for easy mounting. It also includes a DC/DC converter. The EL240.128.45 is easily interfaced using a built-in RAiO RA8835A standard LCD controller. Each of the pixels has an aspect ratio of 1:1 (V:H) and is individually addressable to clearly display high information content graphics and text.

1.1 Features and benefits

- Excellent visual performance
  - High brightness and contrast
  - Wide viewing angle < 179°
  - No compensation needed
- Rapid display response < 1 ms
- Space-efficient mechanical package
- Low EMI emissions
- Extremely rugged and durable
- Low power (3 W)
- Reliable, long operating life with >100,000 MTBF
- Built-in RAiO RA8835A standard LCD controller

2 Installation and handling

Do not drop, bend, or flex the display. Do not allow objects to strike the surface of the display.

CAUTION: The display uses CMOS and power MOS-FET devices. These components are electrostatic-sensitive. Unpack, assemble, and examine this assembly in a static-controlled area only. When shipping, use packing materials designed for protection of electrostatic-sensitive components.

CAUTION: To prevent injury in the event of glass breakage, an impact-resistant shield or a protective overlay should be used on the viewer side of the display.

2.1 Mounting TFEL displays

Properly mounted, TFEL displays can withstand high shock loads as well as severe vibration found in demanding applications. However, the glass panel used in a TFEL display will break if subjected to bending stresses, high impact, or excessive loads.

Stresses are often introduced when a display is mounted into a product. Ideally, the mounting tabs of the display should be the only point of contact with the system. Use a spacer or boss for support; failure to do so will bend the display and cause the glass to break. The instrument enclosure or frame should not flex or distort in such a way that the bending loads might be transferred to the display during use. Mounting surfaces should be flat to within ±0.6 mm (±.025"). Use all the mounting holes provided. Failure to do so will impair the shock and vibration resistance of the final installation.

The EL240.128.45 is a tab-mounted display. Use appropriate length standoffs to assure that screws through the mounting tabs do not introduce bending stresses into the display. Do not deflect the ECB out of its normal plane. The EL240.128.45 mounting tabs are designed for 3 mm screws.

WARNING: These products generate voltages capable of causing personal injury (high voltage up to 230 V_{AC}). Do not touch the display electronics during operation.

2.2 Cable length

A maximum cable length of 600 mm (24 in.) is recommended. Longer cables may cause data transfer problems between the data transmitted and the display input connector. Excessive cable lengths can pick up unwanted EMI.

2.3 Cleaning

As with any glass or coated surface, care should be taken to minimize scratching. Clean the display glass with mild, water-based detergents only. Apply the cleaner sparingly to a soft cloth, then wipe the display. Disposable cleaning cloths are recommended to minimize the risk of inadvertently scratching the display with particles embedded in a re-used cloth. Particular care should be taken when cleaning displays with anti-glare and anti-reflective films.

2.4 Avoiding burn-in

As with other light-emitting displays, displaying fixed patterns on the screen can cause burn-in where luminance variations can be noticed. Use a screensaver or image inversion to avoid causing burn-in on the display.

3 Specifications

The TFEL panel is a matrix structure with column and row electrodes arranged in an X-Y formation. Light is emitted when an AC voltage of sufficient amplitude is applied at a row-column intersection. The display operation is based on the symmetric, line-at-a-time data addressing scheme.

3.1 Power

The supply voltages are shown in Table 1. All internal high voltages are generated from the display supply voltage (V_H). The logic supply voltage (V_L) should be present whenever video input signals are applied. The minimum and maximum specifications in this manual should be met, without exception, to ensure the long-term reliability of the display. Performance characteristics are guaranteed when measured at 25°C with rated input voltage unless otherwise specified. Beneq does not recommend operation of the display outside these specifications.

Table 1. DC input voltage requirements

Description	Name	Min	Typ* (W)	Max	Absolute Max	Units
Input voltage (nom=12.0 V)	V_H	8		18.0		V_{DC}
Input voltage absolute max.	V_H max	--			19.0	V_{DC}
Input current (V_H =12.0 V)	I_H	--		0.95		A_{DC}
Logic voltage (nom=5.0 V)	V_L	4.75		5.25		V_{DC}
Logic voltage absolute max.	V_L max	-0.5			6.0	V_{DC}
Logic current	I_L	--		90		mA_{DC}
Power consumption @ 120 Hz			3.1	5.5		W
Power consumption @ 240 Hz			5.8	10.9		W

*15 % of pixels on per row

CAUTION: Absolute maximum ratings are those values beyond which damage to the device may occur.

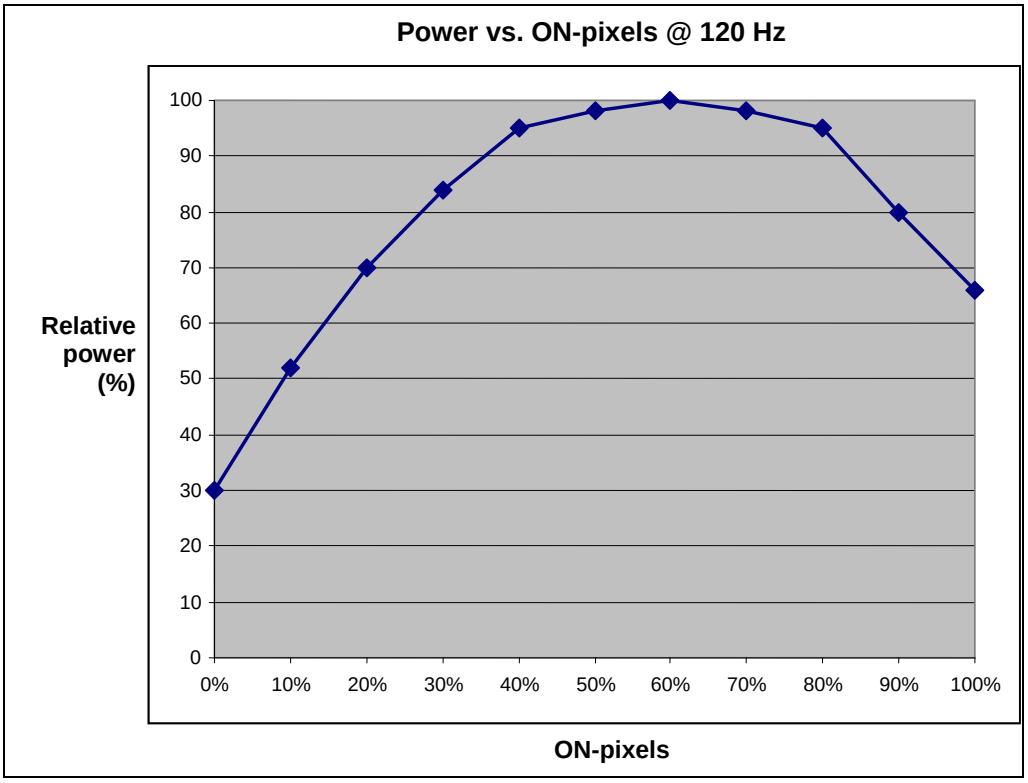


Figure 1. Power curve diagram

Table 2. Video input requirements

Description	Symbol	Min	Max	Units
Absolute Input Voltage Range	VI_{max}	-0.3	V_L + 0.3	V
Low-level input voltage	V_{IL}	0	0.2 x V_L	V
High-level input voltage (except SEL1)	V_{IH}	0.5 x V_L	V_L	V
High-level input voltage SEL1		0.8 x V_L	V_L	
Logic input current*	I_L	–	±10 (-2000)	µA

* Signals /WR, /CS, SEL1, /RD, SELFTEST, /RES have pull-up resistors (4.7 kΩ)

3.2 Connector

Video signals and DC power are supplied to the display through a single 24-pin, dual-row, 2 mm pitch square pin, right-angle, locking connector, such as Samtec part number EHT-112-01-S-D-RA, or an equivalent connector matching the pin outs in Table 3. The mating connector is the Samtec TCSD family of cable strips. Consult your Samtec representative for cable and connector options.

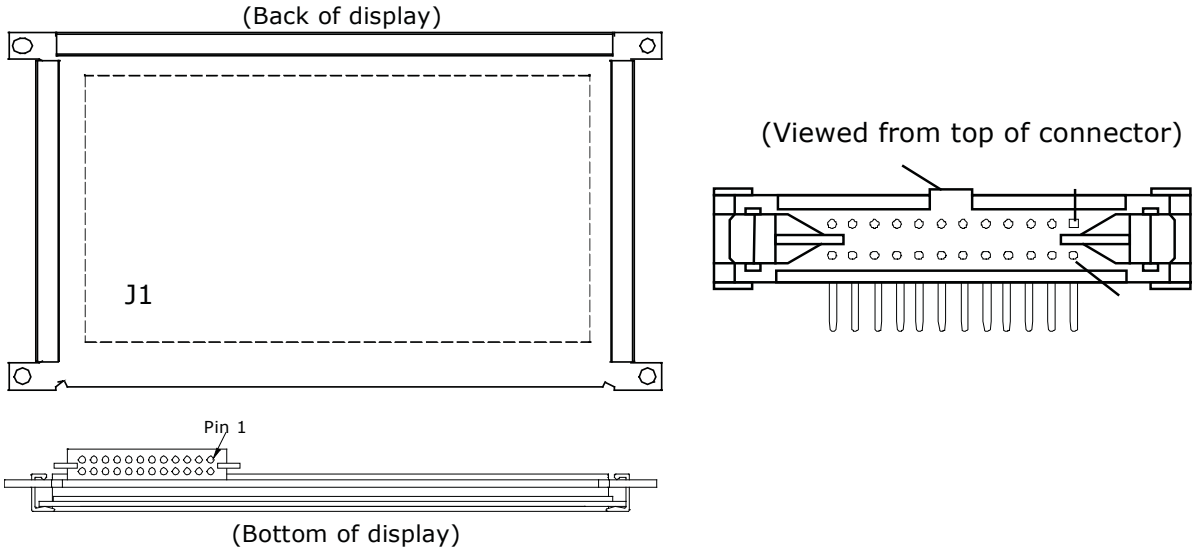


Figure 2. Data/power connector – J1

Table 3. Connector pinouts J1

Pin	Signal	Description	Pin	Signal	Description
1	V_H	Display voltage	2	V_H (+12 V)	
3	GND	Ground	4	GND	Ground
5	V_L (+5 V)	Logic voltage	6	RES	Reset
7	/WR	Write	8	/RD	Read
9	/CS	Chip Select	10	A0	Address
11	SELFTEST		12	GND	Ground
13	D0	input/output	14	D1	input/output
15	D2	input/output	16	D3	input/output
17	D4	input/output	18	D5	input/output
19	D6	input/output	20	D7	input/output
21	SEL1	Select Interface	22	READY	Display ready output
23	GND	Ground	24	LUMA	Luminance control

3.3 Interface information

This Small Graphics Display (SGD) incorporates an interface that is compatible with the 8-bit microprocessor interfaces found in comparable LCD displays with built-in controllers. The display incorporates a built-in RAiO RA8835A standard LCD controller.

Table 4. Pin settings

<table>
<tr><th>Signal</th><th>Functional description</th></tr>
<tr><td>D0 to D7</td><td>Pins 13-20: Tristate input/output pins. Connect to an 8- or 16-bit µP-bus.</td></tr>
<tr><td>SEL1</td><td>Pin 21: µP-interface select. Both 8080-family and 6800-family processors are supported. SEL1 should be tied directly to V_L or GND to prevent noise.
<table>
<tr><th>SEL1</th><th>Interface</th><th>A0</th><th>/RD</th><th>/WR</th><th>/CS</th></tr>
<tr><td>0</td><td>8080 family</td><td>A0</td><td>/RD</td><td>/WR</td><td>/CS</td></tr>
<tr><td>1</td><td>6800 family</td><td>A0</td><td>E</td><td>R//W</td><td>/CS</td></tr>
</table></td></tr>
<tr><td>/RD or E</td><td>Pin 8: With the 8080 interface, this signal acts as the active-LOW read strobe. With the 6800 interface, this signal acts as the active-HIGH enable clock. Data is read from or written to the display when this clock goes HIGH.</td></tr>
<tr><td>/WR or R//W</td><td>Pin 7: With the 8080 interface, this signal acts as the active-LOW write strobe. The bus data is latched on the rising edge of this signal. With the 6800 interface, this signal acts as the read/write control signal. Data is read from the display if this signal is HIGH, and written to the display if it is LOW.</td></tr>
<tr><td>/RES</td><td>Pin 6: When low resets RA8835A, must be high or unconnected in normal operation.</td></tr>
<tr><td>READY</td><td>Pin 22: OUTPUT When data for Row 128 is written to display drivers, this signal goes high. While the signal is high, it is possible to write data to RA8835A memory so that it does not cause disturbances to display data. This signal goes low at the latest 3.5 µs before the loading of Row 1 data begins. Signal READY output is CMOS with 100 Ω series resistor.</td></tr>
<tr><td>/CS</td><td>Pin 9: Chip select. This active-LOW input enables the RA8835A. It is usually connected to the output of an address decoder device that maps the RA8835A into the memory space of the controlling microprocessor.</td></tr>
</table>

<table>
<tr><th>Signal</th><th>Functional description</th></tr>
<tr><td>A0</td><td>Pin 10: A0, in conjunction with the /RD and /WR or R//W and E signals, controls the type of access to the display, as shown below.

8080 Family Interface
<table><tr><th>A0</th><th>/RD</th><th>/WR</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>1</td><td>Status flag read</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Display data and cursor address read</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Display data and parameter write</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Command write</td></tr></table>
6800 Family Interface
<table><tr><th>A0</th><th>/RD</th><th>/WR</th><th>Function</th></tr><tr><td>0</td><td>1</td><td>1</td><td>Status flag read</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Display data and cursor address read</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Display data and parameter write</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Command write</td></tr></table></td></tr>
<tr><td>SELF-TEST</td><td>Pin 11: This pin should be connected to GND for normal display operation. When high, the display operates in the SELFTEST mode.</td></tr>
<tr><td>V_L (+5 V)</td><td>Pin 5: +5 V logic supply voltage.</td></tr>
<tr><td>V_H (+12 V)</td><td>Pins 1 and 2: +12 V supply for DC-DC converter and display analog circuits.</td></tr>
<tr><td>LUMA</td><td>Pin 24: Luminance control input.</td></tr>
<tr><td>GND</td><td>Pins 3, 4, 12, and 23: Signal return for logic and power supplies.</td></tr>
</table>

3.3.1 Video input signals

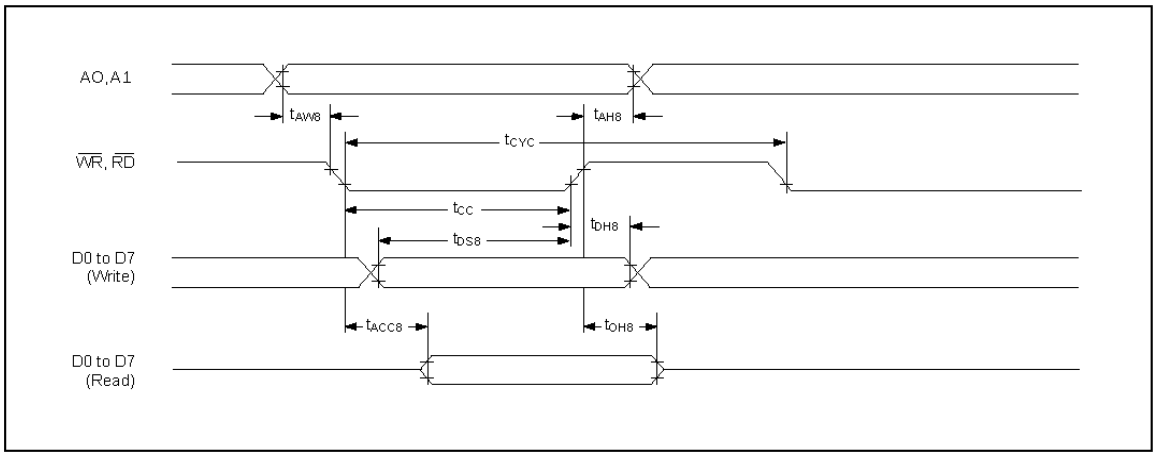


Figure 3. 8080 video input timing diagram

Table 5. 8080 video input timing description

Signal	Symbol	Parameter				Condition
			min	max	unit	
A0, CS	t_{AH8}	Address hold time	10	-	ns	
	t_{AW8}	Address setup time	0	-	ns	
WR, RD	t_{CYC}	System cycle time	550	-	ns	
	t_{CC}	Strobe pulse width	120	-	ns	CL=100 pF
	t_{DS8}	Data setup time	120	-	ns	
D0 to D7	t_{DH8}	Data hold time	5	-	ns	
	t_{ACC8}	RD access time	-	50	ns	
	t_{OH8}	Output disable time	10	50	ns	
All signals	Tr, Tf	Input rise and fall times		30	ns	

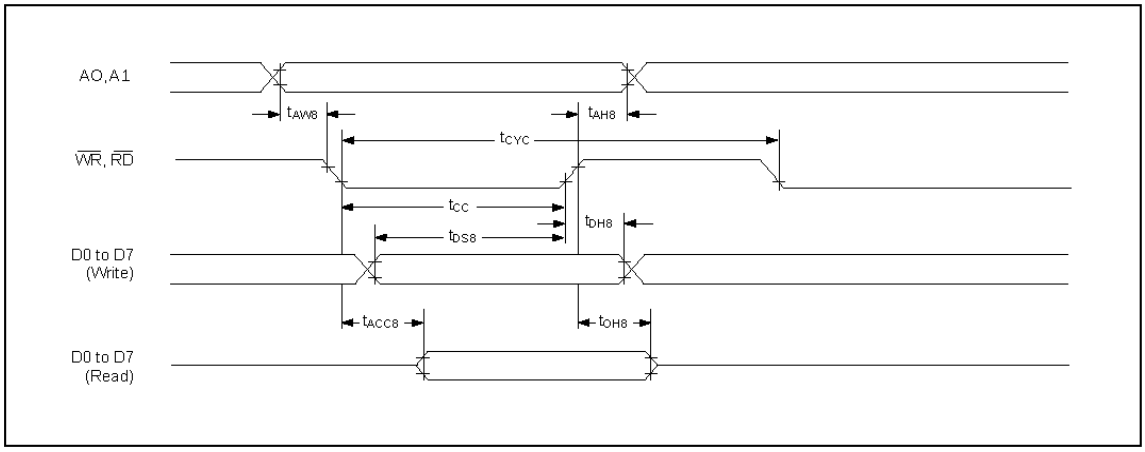


Figure 4. 6800 Video input timing diagram

Table 6. 6800 Video input timing description

Signal	Symbol	Parameter				Condition
			min	max	Unit	
A0, /CS,	t_{CYC6}	System cycle time	550	-	ns	
R//W	t_{AW6}	Address setup time	0			
	t_{AH6}	Address hold time	0	-	ns	
	t_{DS6}	Data setup time	100	-	ns	CL=100 pF
D0 to D7	t_{DH6}	Data hold time	0	-	ns	
	t_{OH6}	Output disable time	10	50	ns	
	t_{ACC6}	Access time	-	85	ns	
E	t_{EW}	Enable pulse width	120			
All signals	Tr, Tf	Input rise and fall times		30	ns	

3.4 Dimming

The dimming control circuitry on the display allows the user to adjust the luminance from 5% to 95% of the maximum brightness.

To control the display luminance, connect a 50 kΩ variable resistor between ground and the dimming pin (LUMA). The full resistance of 50 kΩ will result in 95% of the maximum luminance. Reducing the resistance will reduce the luminance, with resistance of 0 Ω yielding roughly 5% of the maximum luminance.

Alternatively, an external voltage or current-mode D/A converter may be used to dim the display by sinking a maximum of 250 μA for maximum dimming from LUMA to ground. When left open, the luminance will remain at the maximum level.

Table 7. Luminance control

Maximum (no resistor connected): 100 % (Default)
Maximum (50 k Ω resistor connected): 95 %
Minimum (0 Ω resistor connected): 5 % maximum
Open circuit voltage 4 V nominal
Sink current 250 μA max, Vin = 0 V
Luminance values are measured as a percentage of full on luminance (with the external resistor disconnected.)

3.5 Self-test mode

The display incorporates a self-test mode composed of a 1 x 1 checkerboard and full-on pattern displayed at 240 Hz. Upon power up, the 1 x 1 pattern is displayed for several seconds, after which the full-on pattern is displayed continuously. The self-test mode is entered by leaving the SELFTEST pin pulled high. For normal operation, the SELFTEST pin must be pulled to a logic low. If the SELFTEST pin is pulled high during normal operation, the display will enter the self-test mode with the all-pixels-on pattern.

3.6 Power-up sequence

No special power-up or video sequencing is required.

3.7 Optical

Table 8. Optical characteristics

Luminance		
L_{on} (areal), typ	65 cd/m² 130 cd/m²	@ 120 Hz @ 240 Hz
L_{on} (areal), min	45 cd/m² 90 cd/m²	@ 120 Hz @ 240 Hz
L_{off} (areal), max	0.30 cd/m²	@ 240 Hz
Non-uniformity		
All pixels fully lit	25%	Maximum difference between any 2 of 5 points, using the formula: LNU %=[1- (min_lum/max_lum)] x 100 %
Luminance variation (temperature)		
Maximum	±20%	From 25°C to operating temp. extremes; all pixels on.
Luminance variation (time)		
Maximum	< 20%	10,000 hours at 25°C ambient; all pixels on.
Viewing angle		
Minimum	> 160°	
Contrast ratio		
500 lux	55:1 @ 120 Hz frame rate	97:1 @ 240 Hz frame rate
5000 lux	7.1:1 @ 120 Hz frame rate	13:1 @ 240 Hz frame rate

3.8 Command description

The EL240.128.45 display is driven by the RAiO RA8835A controller. For details on using this controller, refer to the Command Description section of the RA8835 manual titled RA8835 Dot Matrix LCD Controller Specification. This document is available on the RAiO website at http://www.raio.com.tw/.

3.8.1 Required register settings and configuration items

- The module uses one 32 k x 8 SRAM for all CG and display memory.
- W/S, bit 3 of the P1 byte of the SYSTEM SET instruction, is set to 0 for a single drive panel.
- DR, bit 7 of the P1 byte of the SYSTEM SET instruction, is set to 0 to turn off the additional output cycle of the shift clock.
- The recommended SYSTEM.SET parameter values for a frame rate of 240 Hz are (P1 through P8) in hex: 32, 07, 07, 1D, 23, 7F, 1E, 00.
- P5 must not be less than 23 to guarantee that minimum line period requirement of the display is achieved (32.5 µs).
- The READY flag is high during extra line times, so P6 should be over 7F if the READY flag is used. After the falling edge of the READY flag, there is min. 3.5 µs time to end the display memory write cycle.
- Oscillator frequency to RAiO RA8835A is 10 MHz.

3.9 Environmental

Table 9. Environmental characteristics

Temperature		
Operating	-40 °C to +70 °C	
Operating survival	-40 °C to +85 °C	
Non-operating	-50 °C to +105 °C	After 12 hours at -50 °C, display must be at -40°C for 1 hour prior to power on.
Humidity		
Operating	to 93 % RH max @ 40 ºC, per IEC 60068-2-78 (non-condensing)	
Non-operating	to 95 % RH max @ 25-55 °C, per IEC 60068-2-30 (condensing)	
Altitude		
Operating/non-operating	0 to 18,000 m per IEC 60068-2-13	
Vibration		
Operating/non-operating	0.02 g^2/Hz, 5-500 Hz, 30 minutes on each axis, per IEC 60068-2-64, Random	
Mechanical shock		
Operating/non-operating	100 g, 6 ms duration (half sine wave), three shocks per surface (6), tested per IEC 60068-2-27, Test Ea	
Thermal shock		
	40 °C for 30 min., room temperature for ~3 min., then 85 °C for 30 min. Cycle repeated five times.	
Displays are non-operating during the tests performed per IEC 60068-2-14. Test Na.		

3.10 Reliability

The display MTBF is demonstrated to be greater than 100,000 hours at maximum frame rate with a 90% confidence level at 25°C.

3.11 Safety and EMI performance

The display will not inhibit the end product from complying with FCC Part 15 Subpart J, Class B and EN55022 Class B when housed in a suitable enclosure.

The display will be a recognized component under UL1950 by Underwriters Laboratories. The display will not inhibit the end product from complying with CSA C22.2 No. 950 and EN60950.

3.12 Mechanical characteristics

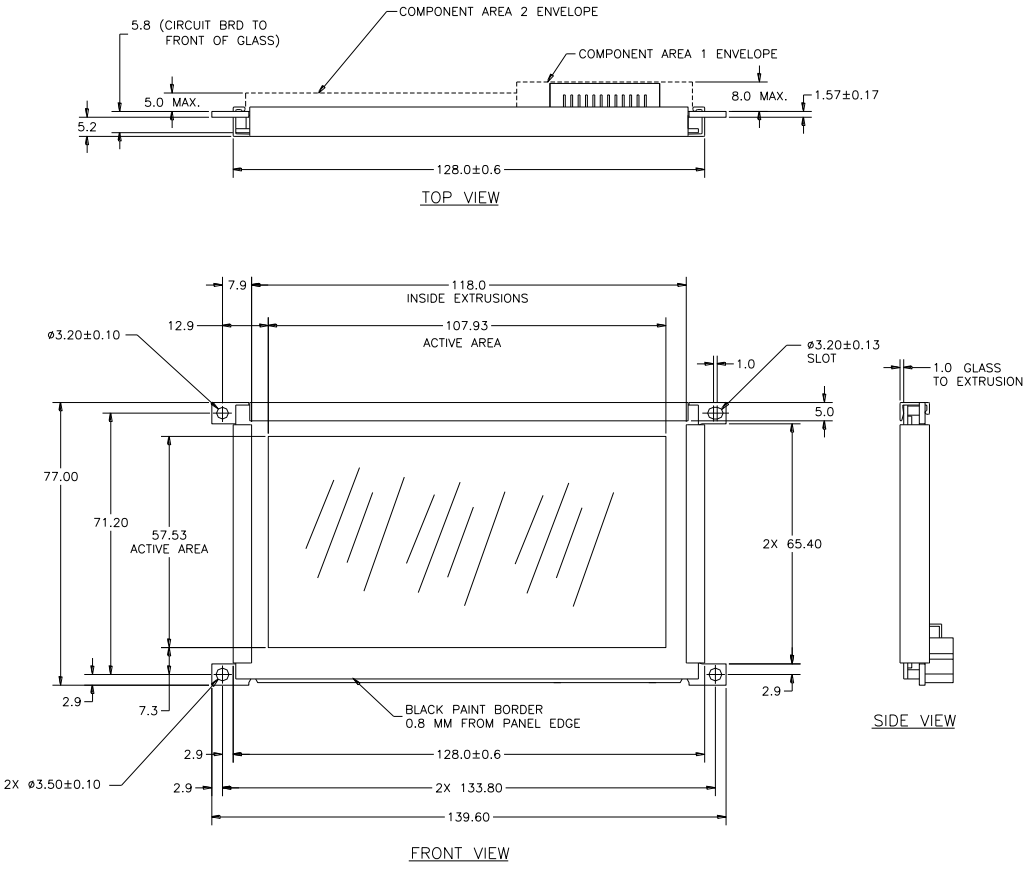
Table 10. Mechanical characteristics

Display external dimensions		
millimeters (inches)	width	128.0 (5.04) nominal ~140.0 mm w/ mounting ears
without locking connector	height	77.0 (3.03) nominal
with locking connector	depth	14.8 (0.59) nominal
Weight	115 g	(4.1 oz) nominal
Fill factor	71.3%	
Display active area		
millimeters (inches)	width	107.9 (4.25) nominal
	height	57.5 (2.26) nominal
	diagonal	122.3 (4.8) nominal
Pixel size		
millimeters (inches)	width	0.38 (0.015)
	height	0.38 (0.015)
Pixel pitch		
millimeters (inches)	horizontal	0.45 (0.018) nominal
	vertical	0.45 (0.018) nominal

3.13 Component envelope

The component envelope shown in Figure 4 illustrates the distance the components extend behind the display. Tall components do not necessarily fill this area. Beneq reserves the right to relocate components within the constraints of the component envelope without prior customer notification. For this reason, Beneq advises users to design enclosure components to be outside the component envelope.

An air gap of at least 5 mm is recommended to dissipate heat from display components. Device designers will need to consider their specific system requirements to determine the necessary spacing.



Dimensions are in millimeters.
Tolerances unless specified:
.x ±0.50
.xx ±0.25

Figure 5. Display dimensions

4 Description of warranty

Seller warrants that the Goods will conform to published specifications and be free from defects in material during warranty time from delivery. To the extent that goods incorporate third-party-owned software, seller shall pass on seller's licensor's warranty to buyer subject to the terms and conditions of seller's license.

Warranty repairs shall be warranted for the remainder of the original warranty period. Buyer shall report defect claims in writing to seller immediately upon discovery, and in any event, within the warranty period. Buyer must return goods to seller within 30 days of seller's receipt of a warranty claim notice and only after receiving seller's return goods authorization. Seller shall, at its sole option, repair or replace the goods.

If goods were repaired, altered or modified by persons other than seller, this warranty is void. Conditions resulting from normal wear and tear and buyer's failure to properly store, install, operate, handle or maintain the goods are not within this warranty. Repair or replacement of goods is seller's sole obligation and buyer's exclusive remedy for all claims of defects. If that remedy is adjudicated insufficient, Seller shall refund buyer's paid price for the goods and have no other liability to buyer.

All warranty repairs must be performed at seller's authorized service center using parts approved by seller. Buyer shall pay costs of sending goods to seller on a warranty claim and seller shall pay costs of returning goods to buyer. The turnaround time on repairs will usually be 30 working days or less. Seller accepts no added liability for additional days for repair or replacement.

If seller offers technical support relating to the goods, such support shall neither modify the warranty nor create an obligation of seller. Buyer is not relying on seller's skill or judgment to select goods for buyer's purposes. Seller's software, if included with goods, is sold as is, and this warranty is inapplicable to such software.

SELLER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

5 Ordering information

Product	Part number	Features
EL240.128.45	996-0301-01LF	Standard version
EL240.128.45 CC	996-0301-03LF	Conformal coating

Design and specifications are subject to change without notice.

Beneq continues to provide optional, and in many cases custom, features to address the specific customer requirements. Consult Beneq Sales for pricing, lead time and minimum quantity requirements.

6 Support and service

Beneq Oy is a Finnish company based in Espoo, Finland, with a world-wide sales distribution network. Full application engineering support and service are available to make the integration of Lumineq displays as simple and quick as possible for our customers.

RMA Procedure: For a Returned Material Authorization number, please contact Beneq Oy by email (rma.lumineq@beneq.com) with the model number(s), serial number(s) and brief description of the problem. When returning goods for repair, please include a brief description of the problem, and mark the outside of the shipping container with the RMA number.

7 RoHS II

Beneq Oy is committed to continuous improvement. As part of this process we are fully in support of EU directive 2011/65/EU, the Restriction of Hazardous Substances, commonly known as RoHS II or RoHS Recast, which, compared to RoHS, keeps the restrictions on the original six hazardous substances, including lead (Pb) in electronic equipment. It also expands these restrictions to previously exempted categories including medical devices and monitoring and control instruments.

Beneq part number with an "LF" suffix designation indicates RoHS compliance, as shown on the part number label affixed to the display and on the box containing the display.