# IB995

## Intel® 8th or 9th Gen. Xeon. Core™ i7/i5/i3 Full-Size CPU Card

# User's Manual

Version 1.1a
(Sep. 2021)

## Compliance

CE

In a domestic environment, this product may cause radio interference in which case users may be required to take adequate measures.

FC

This product has been tested and found to comply with the limits for a Class A device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications.

### WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

### Green IBASE


This product is compliant with the current RoHS restrictions and prohibits use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

# Important Safety Information

Carefully read the precautions before using the board.

### Environmental conditions:

- Use this product in environments with ambient temperatures between 0˚C and 60˚C.
- Do not leave this product in an environment where the storage temperature may be below -20° C (-4° F) or above 80° C (176° F). To prevent from damages, the product must be used in a controlled environment.

**WARNING**

### Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on this product.
- Do not place heavy objects on the top of this product.

### Anti-static precautions

- Wear an anti-static wrist strap to avoid electrostatic discharge.
- Place the PCB on an anti-static kit or mat.
- Hold the edges of PCB when handling.
- Touch the edges of non-metallic components of the product instead of the surface of the PCB.
- Ground yourself by touching a grounded conductor or a grounded bit of metal frequently to discharge any static.

**CAUTION**

Danger of explosion if the internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions or recycle them at a local recycling facility or battery collection point.

## Warranty Policy

- **IBASE standard products:**

  24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

  12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, CPU cooler, memory, storage devices, power adapter, panel and touchscreen.

* PRODUCTS, HOWEVER, THAT FAIL DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

## Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If you need any further assistance from your distributor or sales representative, prepare the following information of your product and elaborate upon the problem.
   - Product model name
   - Product serial number
   - Detailed description of the problem
   - The error messages in text or in screenshots if there is any
   - The arrangement of the peripherals
   - Software in use (such as OS and application software, including the version numbers)
3. If repair service is required, you can download the RMA form at http://www.ibase.com.tw/english/Supports/RMAService/. Fill out the form and contact your distributor or sales representative.

# Table of Contents

# Chapter 1
# General Information

The information provided in this chapter includes:

- Features
- Packing List
- Optional Accessories
- Block Diagram
- Specifications
- Board View
- Board Dimensions

## 1.1 Introduction

The IB995AF PICMG1.3 SHB Express CPU Card is based on the latest 8th or 9th Gen. Intel® Xeon® E / Core™ / Pentium® / Celeron® processor with speeds of up to 4.7GHz and features an integrated graphics core that work with LVDS, DVI-I and DVI-D display outputs.

IB995 utilizes the dramatic increase in performance provided by Intel's latest cutting-edge technology. Measuring 338mm x122mm, IB995 offers fast 6Gbps SATA support (up to 8 ports), USB3.1 (5 ports) and interfaces for two Gigabit LAN.

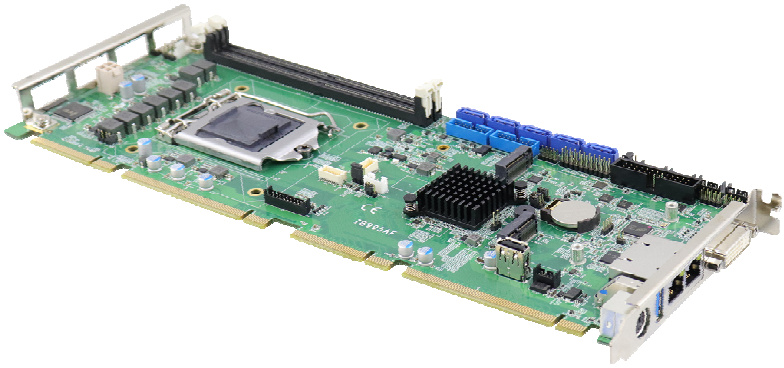


**Photo of IB995**

## 1.2 Features

- 2 x DDR4-2400/2666 UDIMM, expandable up to 32GB, ECC supported per CPU SKUS.
- Dual Gigabit LAN
- 1 x DVI-I , 1 x DVI-D, 1 x 24-bit dual channel LVDS
- 5 x USB 3.1, 8 x SATA III, 4 x serial ports
- PCIe (x16), M.2 M2280 (for IB995AF series only) and M.2 E2230 expansion slots
- Configurable watchdog timer, digital I/O, TPM

## 1.3 Packing List

Your IB995 package should include the items listed below. If any of the items is missing, please contact the distributor or dealer from whom you have purchased the product.

- IB995AF PICMG1.3 SHB x 1
- I/O shield
- SATA cable (SATA-5)
- COM port cable (PK1-150)
- Disk (including chipset drivers)
- This user's manual

## 1.4 Optional Accessories

- Audio cable (Audio-18)
- DVI-D cable (DVIK-3)
- USB cable (USB-29)
- USB3.0 cable (USB-3K)
- Printer port cable (PK3K)

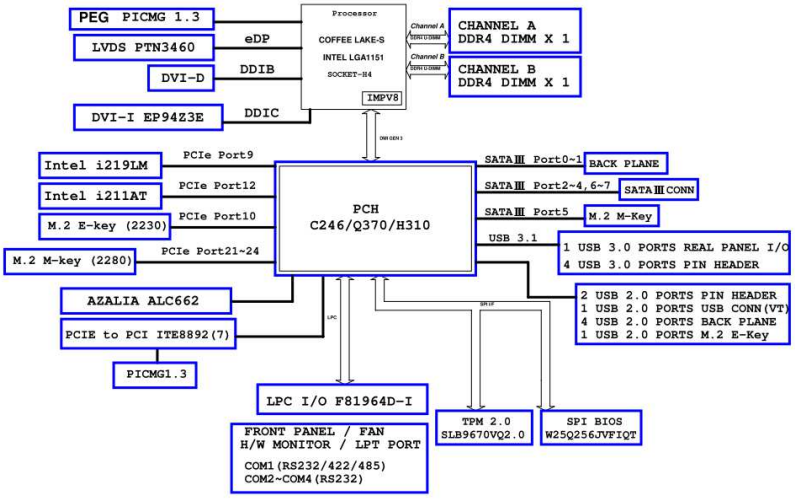
## 1.5 Specifications

| Product Name | IB995AF Series | IB995EF |
|---|---|---|
| **Form Factor** | PICMG 1.3 SHB Express full size CPU card | |
| **System** | | |
| **Operating System** | • Microsoft Windows 10 (64-bit)<br>• Linux Ubuntu (64-bit) | |
| **CPU & Chipset** | 9th / 8th Gen. Intel® Xeon® E / Core™ / Pentium® / Celeron®, up to 4.7 GHz | |
| **Memory** | 2 x DDR4 UDIMM 2666 / 2400 MHz, up to 32 GB<br>* ECC will be supported by identified CPU SKUs. | |
| **Storage** | M.2 M2280 slot (NVMe supported) | N/A |
| **Graphics** | Intel® UHD Graphics P630 | |
| **LAN** | 1st LAN: Intel® I219LM GbE<br>2nd LAN: Intel® I210AT / I211AT GbE | 1st LAN: Intel® I219V GbE<br>2nd LAN: Intel® I211AT GbE |
| **Security** | TPM 2.0 | |
| **Super I/O** | Fintek F81964D-I | |
| **Digital I/O** | 4-In / 4-Out | |
| **Audio Codec** | Built HD audio with Realtek ALC662 | |
| **Watchdog Timer** | Yes (256 segments, 0, 1, 2…255 sec / min) | |
| **BIOS** | AMI BIOS | |
| **iSmart** | N/A | |
| **RAID** | RAID 0/1/5 | N/A |
| **iAMT** | 11.6 (with E-Xeon® / Core i7/ i5 DT CPU SKUs) | N/A |
| **TPM** | 2.0 | |
| **Dimensions** | 338mm x 126mm | |
| **RoHS** | Yes | |
| **Certification** | CE, FCC | |

| Model | IB995AF Series | IB995EF |
|---|---|---|
| **I/O Ports** | | |
| **Display** | • 1 x DVI-D (1920 x 1080 at 60 Hz)<br>• 1 x DVI-I (1920 x 1080 at 60 Hz)<br>• 1 x 24-bit dual channel LVDS (1920 x 1080 at 60 Hz) | |
| **LAN** | • 2 x RJ45 GbE LAN<br>• 1 x M.2 (E-key@2230), Support CNVi | |
| **USB** | • 1 x USB 3.1 (I/O coastline connectors)<br>• 4 x USB 3.1 (via two onboard pin-header)<br>• 1 x USB 2.0 ports (via M.2 E2230)<br>• 1 x USB 2.0 (Vertical type A)<br>• 2 x USB 2.0 (via an onboard pin-header)<br>• 4 x USB 2.0 to Backplane | • 1 x USB 3.1 (I/O coastline connectors)<br>• 1 x USB 2.0 (Vertical type A)<br>• 4 x USB 2.0 to Backplane |
| **Serial** | **4 x COM ports:**<br>• COM1: RS-232/422/485 (Support Ring-in with power at 500mA, selectable for 5V or 12V)<br>• COM2 ~ COM4: RS-232 only (via onboard box-headers) | **4 x COM ports:**<br>• COM1: RS-232/422/485 (Support Ring-in with power at 500mA, selectable for 5V or 12V)<br>• COM2 ~ COM4: RS-232 only (via onboard box-headers)) |
| **SATA** | • IB995AF-C246 support 8 ports, 5 x SATAIII (3.0) 6Gbps<br>• IB995AF(Q370) support 6 ports, 3 x SATAIII (3.0) 6Gbps<br>• IB995EF(H310); support 4 ports, 2 x SATAIII (3.0) 6Gbps | |
| **Digital IO** | 4-In & 4-Out | |
| **Expansion Slots** | • 1 x PCIe (x16)<br>• 1 x M.2 M2280<br>• 1 x M.2 E2230 | • 1 x PCIe (x16)<br>• 1 x M.2 E2230 |
| **Environment** | | |
| **Temperature** | • **Operating:** 0 ~ 60 °C (32 ~ 140 °F)<br>• **Storage:** -20 ~ 80 °C (-4 ~ 176 °F) | |
| **Relative Humidity** | 0 ~ 90 %, non-condensing at 60 °C | |

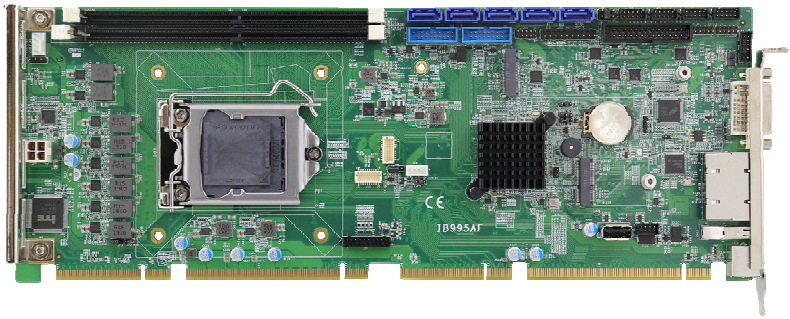
All specifications are subject to change without prior notice.

## 1.6 Block Diagram

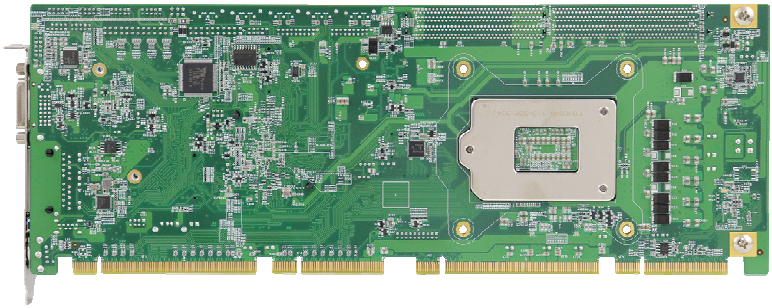


## 1.7 Board Pictures

### Top View



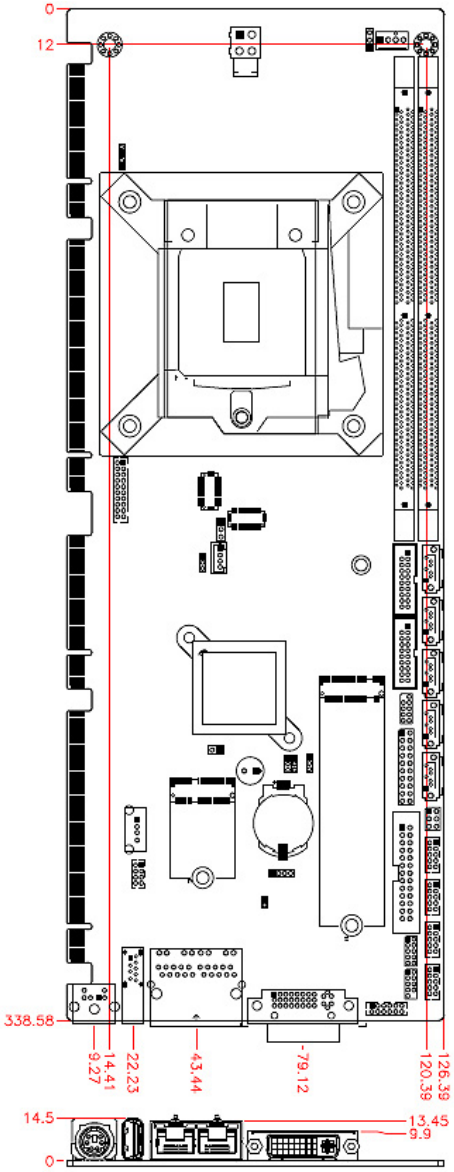
### Bottom View



### I/O View

* The photos above are for reference only.

## 1.8 Dimensions



# Chapter 2
# Hardware Configuration

This section provides information on jumper settings and connectors on the IB995 in order to set up a workable system. On top of that, you will also need to install crucial pieces such as the CPU and the memory before using the product. The topics covered are:

- Essential installations
- Jumper and connector locations
- Jumper settings and information of connectors

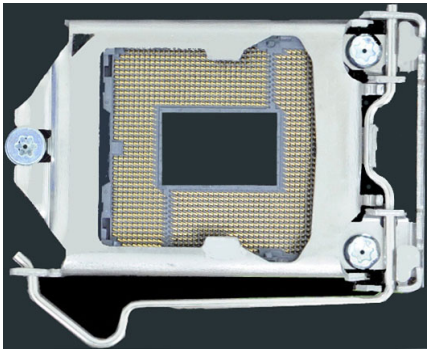
## 2.1 Essential Installations Before You Begin

Follow the instructions below to install the CPU and the memory.

### 2.1.1 Installing the CPU

The IB995 board supports an LGA1151 Socket (shown below) for Intel® Xeon® E3 v5 family or Intel® 6th Gen. Core™ i7 / i5 / i3 DT processor processors. Follow the instructions below to install the CPU.

1. Unlock the socket by pressing the lever sideways, then lift up the lever and the metal lid.
2. Position the CPU above the socket such that the CPU corner aligns with the gold triangle matching the socket corner with a small triangle.
3. Carefully insert the CPU into the socket and push down the lever to secure the CPU.

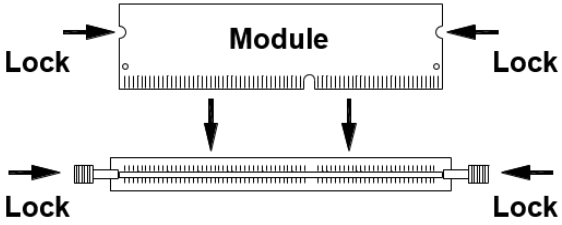


Then you can install the CPU cooler and fan.

**Note:** Ensure that the CPU cooler and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.

### 2.1.2 Installing the Memory

The IB995 board supports two DDR4 memory socket for a maximum total memory of 32GB in DDR4 UDIMM memory type. To install the modules, locate the memory slot on the board and perform the following steps:




1. Hold the module so that the key of the module aligned with that on the memory slot.
2. Gently push the module in an upright position until the clips of the slot close to hold the module in place when the module touches the bottom of the slot.

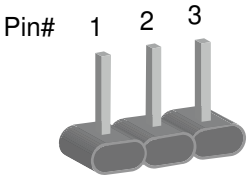
To remove the module, press the clips outwards with both hands

## 2.2 Setting the Jumpers

Set up and configure your IB995 by using jumpers for various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your use.

### 2.2.1 How to Set Jumpers

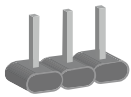
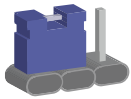
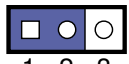
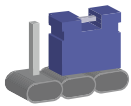
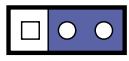
Jumpers are short-length conductors consisting of several metal pins with a non-conductive base mounted on the circuit board. Jumper caps are used to have the functions and features enabled or disabled. If a jumper has 3 pins, you can connect either PIN1 to PIN2 or PIN2 to PIN3 by shorting.




**A 3-pin jumper**

**A jumper cap**

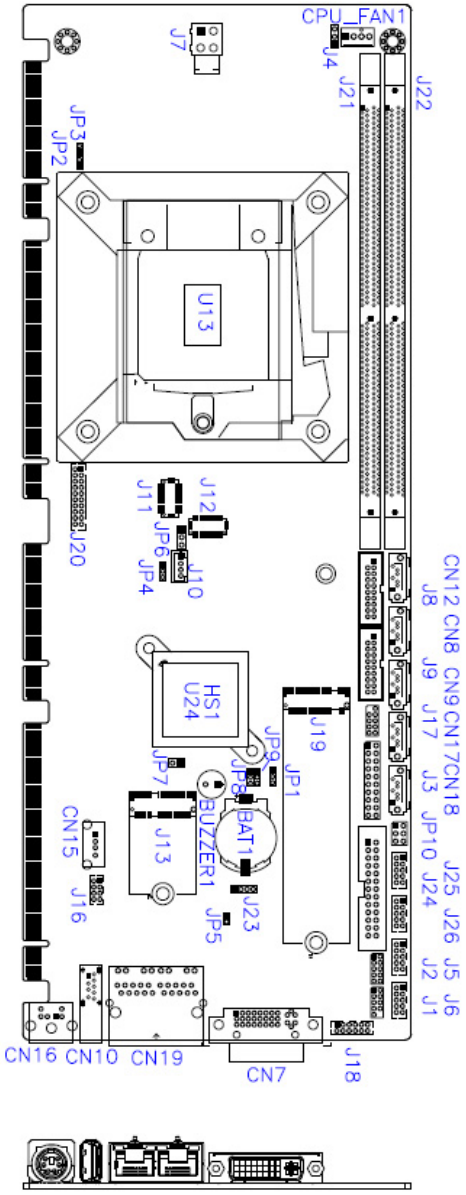
Refer to the illustration below to set jumpers.

| Pin closed | Oblique view | Illustration |
|---|---|---|
| Open |  |   |
| 1-2 |  |   |
| 2-3 |  |   |

When two pins of a jumper are encased in a jumper cap, this jumper is **closed**, i.e. turned **On**.

When a jumper cap is removed from two jumper pins, this jumper is **open**, i.e. turned **Off**.

## 2.3 Jumper & Connector Locations on IB995

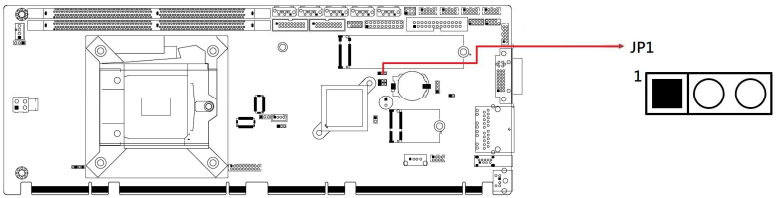


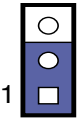
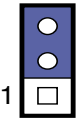

**Board diagram of IB995AF (for Q170)**

## 2.4 Jumpers Quick Reference

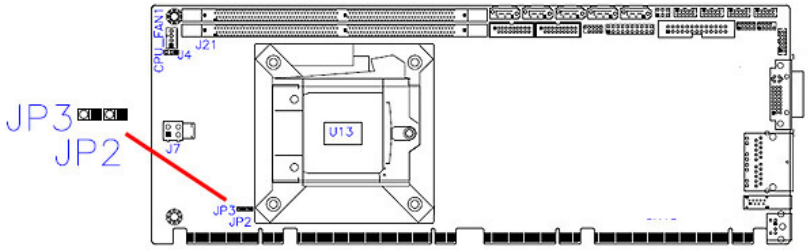
| Function | Jumper | Page |
|---|---|---|
| ATX/AT Power Mode Selection | JP1 | 14 |
| PCIe Bifurcation Selection | JP2, JP3 | 15 |
| LVDS Panel Brightness Selection | JP4 | 16 |
| LVDS Panel Power Selection | JP6 | 16 |
| Clear ME Register | JP8 | 17 |
| Clear CMOS Data | JP9 | 17 |

### 2.4.1 ATX / AT Power Mode Selection (JP1)



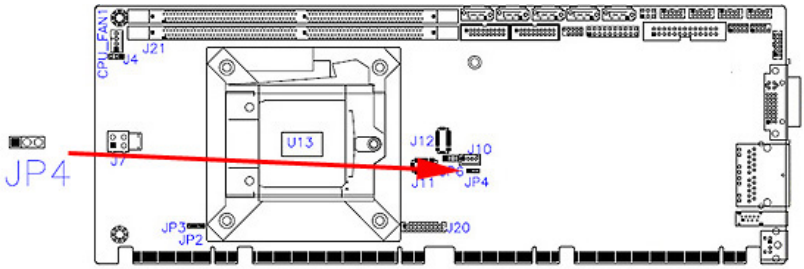

| Function | Pin closed | Illustration |
|---|---|---|
| ATX Mode (default) | 1-2 |   |
| AT Mode | 2-3 |   |

### 2.4.2 PCIe (x16) Bifurcation Selection (JP2 & JP3)



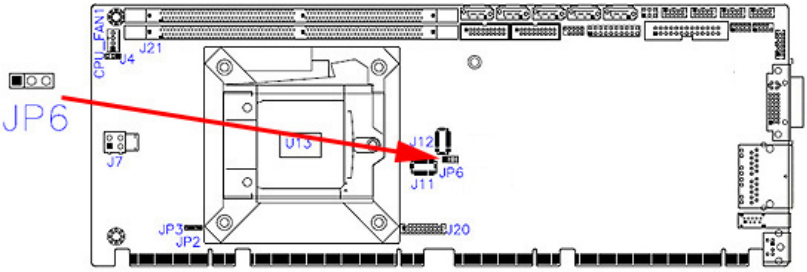

| Function | Pin closed | Illustration |
|---|---|---|
| 1 x PCIe (x16) (default) | **JP3:** Open | 1 |
| | **JP2:** Open | 1 |
| 2 x PCIe (x8) | **JP3:** Open | 1 |
| | **JP2:** Close | 1 |
| 1 x PCIe (x8) 2 x PCIe (x4) | **JP3:** Close | 1 |
| | **JP2:** Close | 1 |

### 2.4.3 LVDS Power Brightness Selection (JP4)



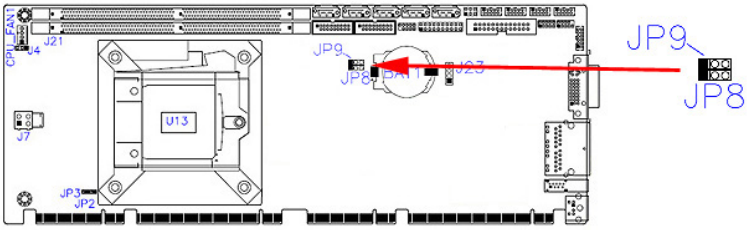

| Function | Pin closed | Illustration |
|---|---|---|
| 3.3V (default) | 1-2 | 1 |
| 5V | 2-3 | 1 |

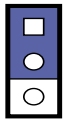
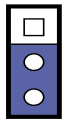
### 2.4.4 LVDS Panel Power Selection (JP6)



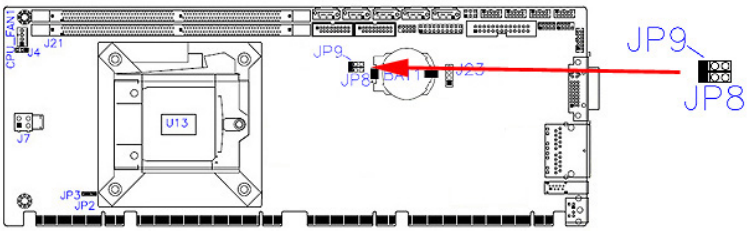

| Function | Pin closed | Illustration |
|---|---|---|
| 3.3V (default) | 1-2 | 1 |
| 5V | 2-3 | 1 |

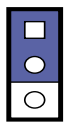
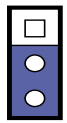
### 2.4.5 Clear ME Register (JP8)




| Function | Pin closed | Illustration |
|---|---|---|
| Normal (default) | 1-2 |  |
| Clear ME | 2-3 |  |

### 2.4.6 Clear CMOS Data (JP9)

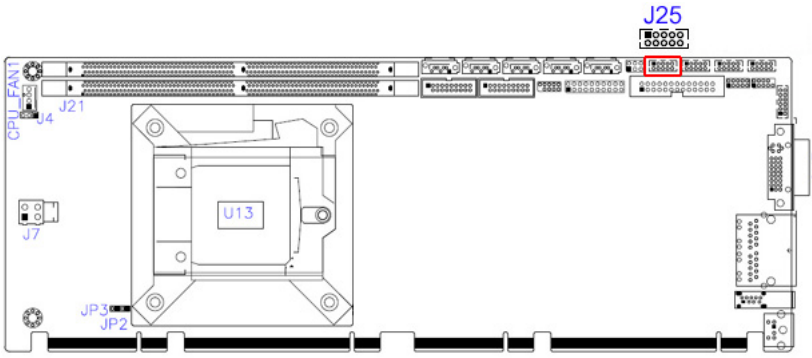



| Function | Pin closed | Illustration |
|---|---|---|
| Normal (default) | 1-2 |  |
| Clear CMOS | 2-3 |  |

## 2.5 Connectors Quick Reference

| Function | Connector Name | Page |
|---|---|---|
| COM1 RS-232/422/485 Ports | J25 | 19 |
| COM2~COM4 RS-232 Ports | J26 (COM2), J5 (COM3), J6 (COM4) | 20 |
| Digital I/O Connector | J2 | 21 |
| LCD Backlight Connector | J10 | 21 |
| ATX 12V Power Connector | J7 | 22 |
| Dual USB 3.0 Pin-Header | J8,J9 | 23 |
| Dual USB 2.0 Pin-Header | J16 | 24 |
| Front Panel Audio Connector | J18 | 25 |
| Front Panel Settings Connector | J3 | 25 |
| LVDS Connector | J11, J12 | 26 |
| Fan Power Connector | CPU_FAN1 | 27 |
| DVI-D Connector | J20 | 28 |
| Parallel Port | J24 | 29 |

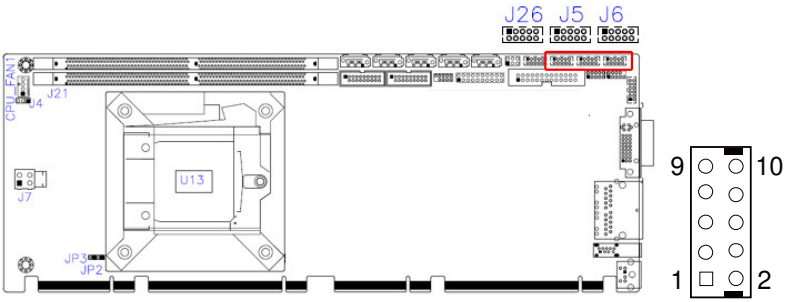
### 2.5.1 COM1 RS-232/422/485 & COM2 RS-232 Serial Port (J25)




| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | DCD, Data carrier detect | 2 | RXD, Receive data |
| 3 | TXD, Transmit data | 4 | DTR, Data terminal ready |
| 5 | Ground | 6 | DSR, Data set ready |
| 7 | RTS, Request to send | 8 | CTS, Clear to send |
| 9 | RI, Ring indicator | 10 | N/A |

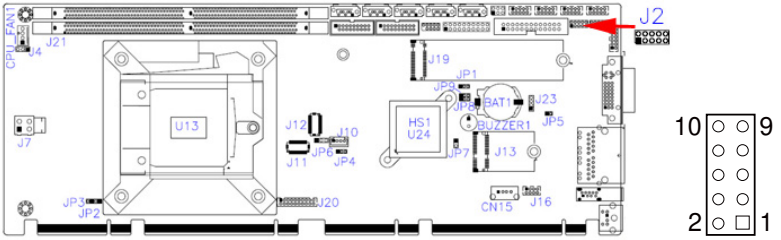
| Pin | Signal Name | | |
|---|---|---|---|
| | RS-232 | RS-422 | RS-485 |
| 1 | DCD | TX- | DATA- |
| 2 | RX | TX+ | DATA+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | Ground | Ground | Ground |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |

### 2.5.2 COM2~COM4 RS-232 Ports (J26, J5, J6)



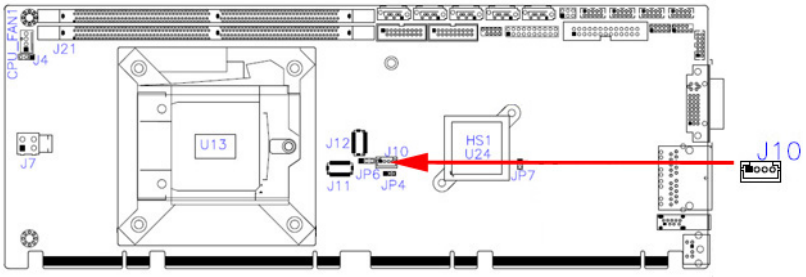

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | DCD, Data carrier detect | 2 | RXD, Receive data |
| 3 | TXD, Transmit data | 4 | DTR, Data terminal ready |
| 5 | Ground | 6 | DSR, Data set ready |
| 7 | RTS, Request to send | 8 | CTS, Clear to send |
| 9 | RI, Ring indicator | 10 | Key |

### 2.5.3 Digital I/O Connector (J2)



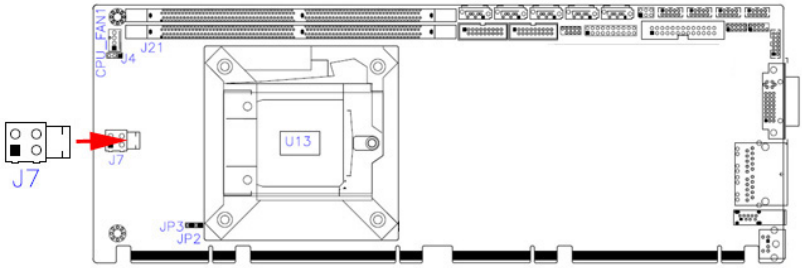

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Ground | 2 | +5V |
| 3 | OUT3 | 4 | OUT1 |
| 5 | OUT2 | 6 | OUT0 |
| 7 | IN3 | 8 | IN1 |
| 9 | IN2 | 10 | IN0 |

### 2.5.4 LCD Backlight Connector (J10)



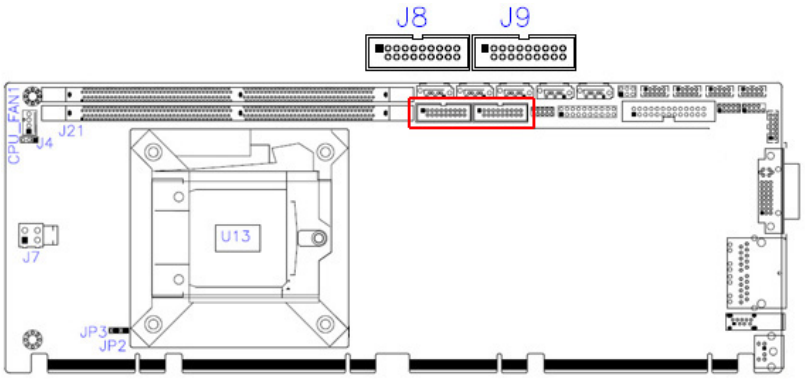

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +12V | 3 | Brightness Control |
| 2 | Backlight Enable | 4 | Ground |

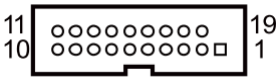
### 2.5.5 ATX Power Connector (J7)




| Pin | Assignment | Pin | Assignment |
|---|---|---|---|
| 1 | Ground | 3 | +12V |
| 2 | Ground | 4 | +12V |

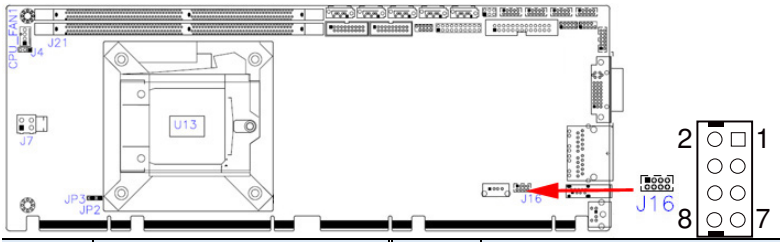
### 2.5.6 USB3.0/2.0 Connector (J8, J9)



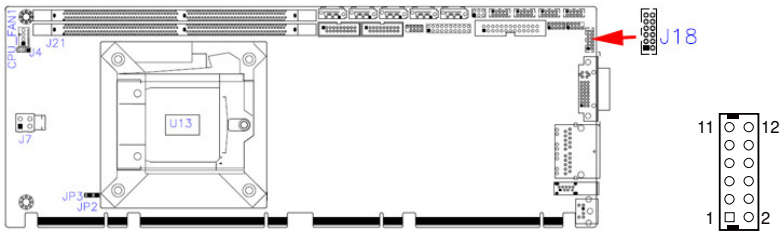

| Pin # | Assigment | Pin # | Assigment |
|---|---|---|---|
| 1 | VCC(900mA) | 11 | P2_U2_D+ |
| 2 | P1_SSRX- | 12 | P2_U2_D- |
| 3 | P1_SSRX+ | 13 | GND |
| 4 | GND | 14 | P2_SSTX+ |
| 5 | P1_SSTX- | 15 | P2_SSTX- |
| 6 | P1_SSTX+ | 16 | GND |
| 7 | GND | 17 | P2_SSRX+ |
| 8 | P1_U2_D- | 18 | P2_SSRX- |
| 9 | P1_U2_D+ | 19 | VCC(900mA) |
| 10 | NC | | |

### 2.5.7 Dual USB 2.0 Connector (J16)



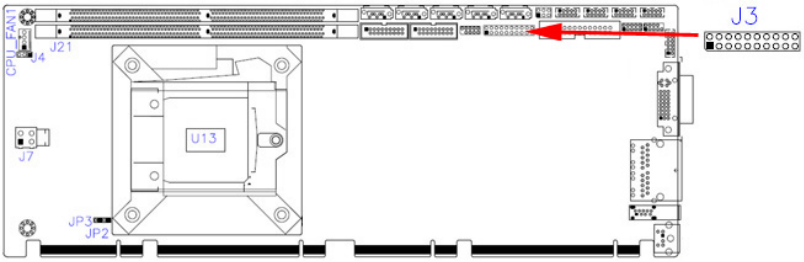

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | VCC | 2 | Ground |
| 3 | D0- | 4 | D1+ |
| 5 | D0+ | 6 | D1- |
| 7 | Ground | 8 | VCC |

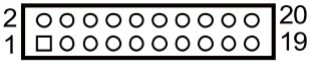
### 2.5.8 Front Panel Audio Connector (J18)




| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | HPOUT_L | 2 | HPOUT_R |
| 3 | HPOUT_JD | 4 | Ground |
| 5 | LINE_L | 6 | LINE_R |
| 7 | LINE_JD | 8 | Ground |
| 9 | MIC IN_L | 10 | MIC IN_R |
| 11 | MIC IN_JD | 12 | Ground |

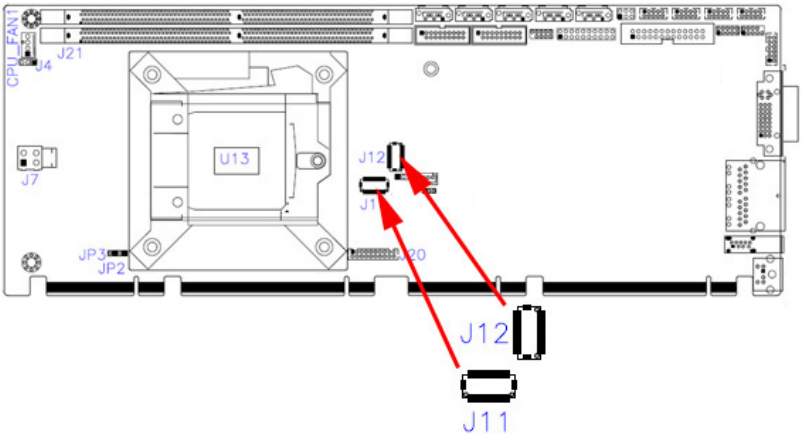
### 2.5.9 Front Panel Settings Connector (J3)




| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | VCC5 | 2 | Speak Out |
| 3 | NC | 4 | NC |
| 5 | Ground | 6 | Ground |
| 7 | NC | 8 | VCC5 |
| 9 | Ground | 10 | NC |
| 11 | Ground | 12 | NC |
| 13 | Power BTN- | 14 | Power BTN+ |
| 15 | System LED+ | 16 | System LED- |
| 17 | Reset BTN- | 18 | Reset BTN+ |
| 19 | HDD LED+ | 20 | HDD LED- |

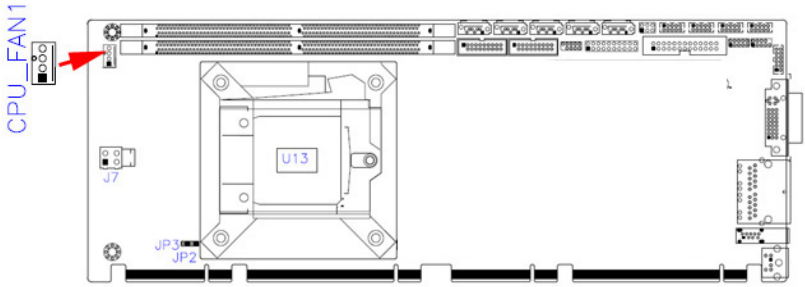
### 2.5.10 LVDS Connector (J11, J12)




| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | TX0P | 2 | TX0N |
| 3 | Ground | 4 | Ground |
| 5 | TX1P | 6 | TX1N |
| 7 | Ground | 8 | Ground |
| 9 | TX2P | 10 | TX2N |
| 11 | Ground | 12 | Ground |
| 13 | CLKP | 14 | CLKN |
| 15 | Ground | 16 | Ground |
| 17 | TX3P | 18 | TX3N |
| 19 | VDD | 20 | VDD |

*Remarks: J11 is 1st LVDS; J12 is 2nd LVDS.*

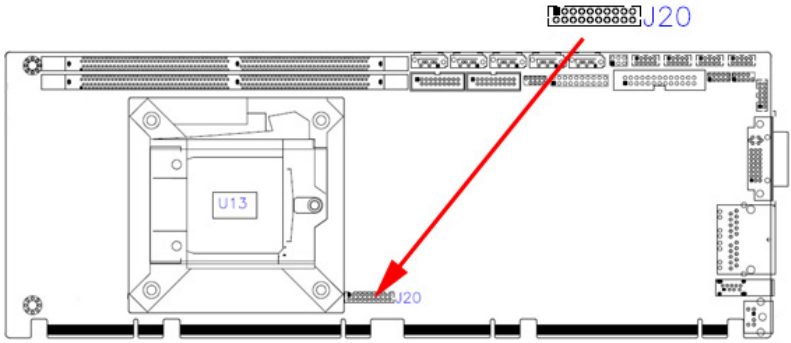
### 2.5.11 Fan Power Connector (CPU_FAN1)

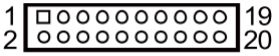



| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Ground | 3 | Rotation detection |
| 2 | +12V | 4 | Control |

*Remarks: (PWM Mode Only)*

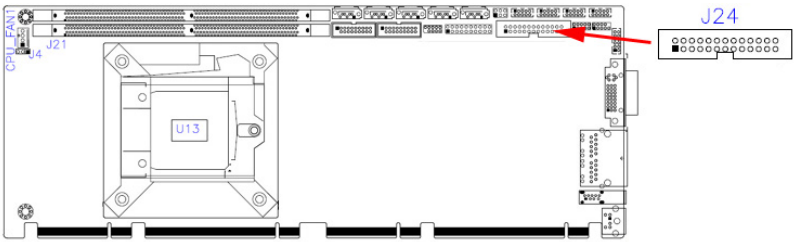
### 2.5.12 DVI-D Connector (J20)

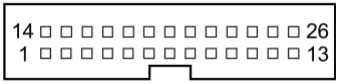



| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | TMDS_DATA1_P | 2 | TMDS_DATA1_N |
| 3 | Ground | 4 | Ground |
| 5 | TMDS_CLK_P | 6 | TMDS_CLK_N |
| 7 | Ground | 8 | Ground |
| 9 | Hot Plug Detect | 10 | NC |
| 11 | TMDS_DATA2_P | 12 | TMDS_DATA2_N |
| 13 | Ground | 14 | Ground |
| 15 | TMDS_DATA0_P | 16 | TMDS_DATA0_N |
| 17 | NC | 18 | NC |
| 19 | TMDS_SDA | 20 | TMDS_SCL |

### 2.5.13 Parallel Port (J24)




| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Line printer strobe | 14 | Auto Feed |
| 2 | PD0, parallel data 0 | 15 | Error |
| 3 | PD1, parallel data 1 | 16 | Initialize |
| 4 | PD2, parallel data 2 | 17 | Select-Printer / Select-In |
| 5 | PD3, parallel data 3 | 18 | Ground |
| 6 | PD4, parallel data 4 | 19 | Ground |
| 7 | PD5, parallel data 5 | 20 | Ground |
| 8 | PD6, parallel data 6 | 21 | Ground |
| 9 | PD7, parallel data 7 | 22 | Ground |
| 10 | ACK,acknowledge | 23 | Ground |
| 11 | Busy | 24 | Ground |
| 12 | Paper Empty | 25 | Ground |
| 13 | Select | 26 | Ground |

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# Chapter 3
# Drivers Installation

This chapter introduces installation of the following drivers:

- Intel® Chipset Software Installation Utility
- VGA Driver
- HD Audio Driver
- LAN Driver
- Intel® Management Engine Interface
- Intel® USB 3.0 Driver

## 3.1 Introduction

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find anything missing, please contact the distributor where you made the purchase. The contents of this section include the following:

---

**Note:** After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

---

## 3.2 Intel® Chipset Software Installation Utility

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for Intel chipset components. Follow the instructions below to complete the installation.

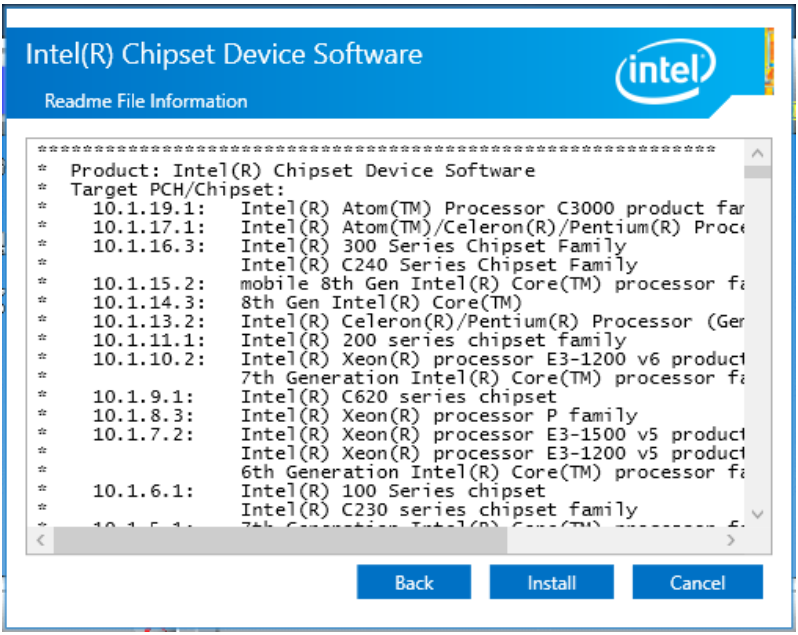
1. Insert the disk enclosed in the package with the board. Click **Intel** and then **Intel(R) Coffeelake Chipset Drivers**.


2. Click Intel(R) Chipset Software Installation Utility.

3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next** to continue.

4. Click **Accept** to accept the software license agreement and proceed with the installation process.

5. On the *Readme File Information* screen, click **Install**.



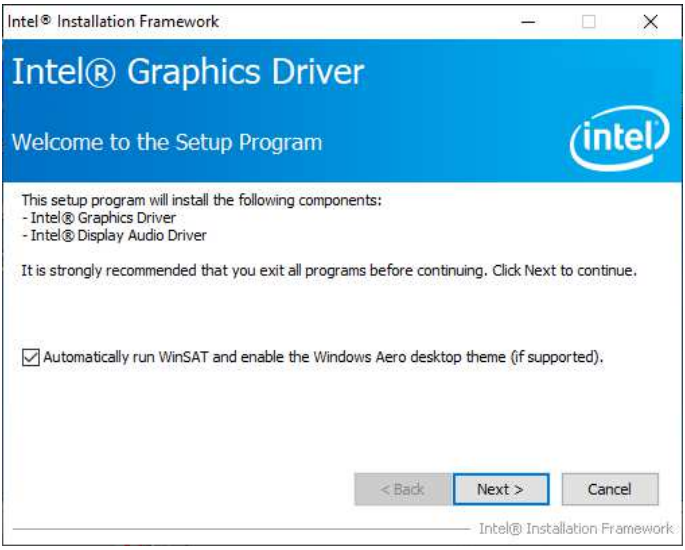

6. When installation is complete, click **Restart Now** to restart the computer and for changes to take effect.

## 3.3 VGA Driver Installation

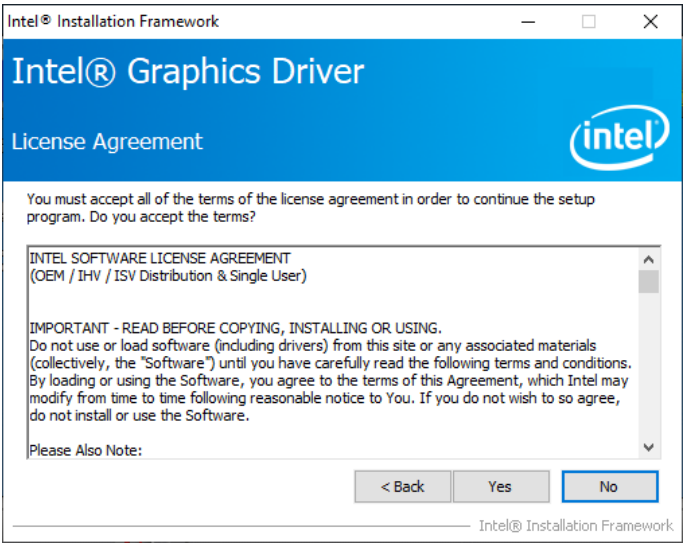
1. Insert the disk enclosed in the package with the board. Click **Intel** and then **Intel(R) Coffeelake Chipset Drivers**.


2. Click **Intel(R) HD Graphics Driver**.

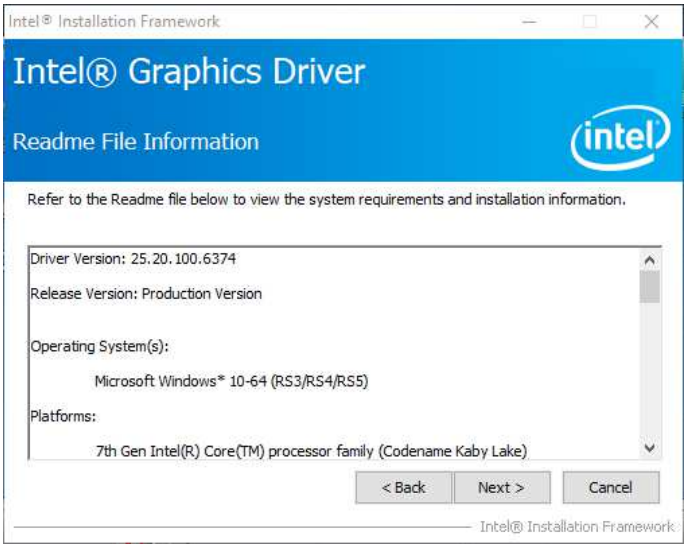
3. When the *Welcome* screen appears, click **Next** to continue.



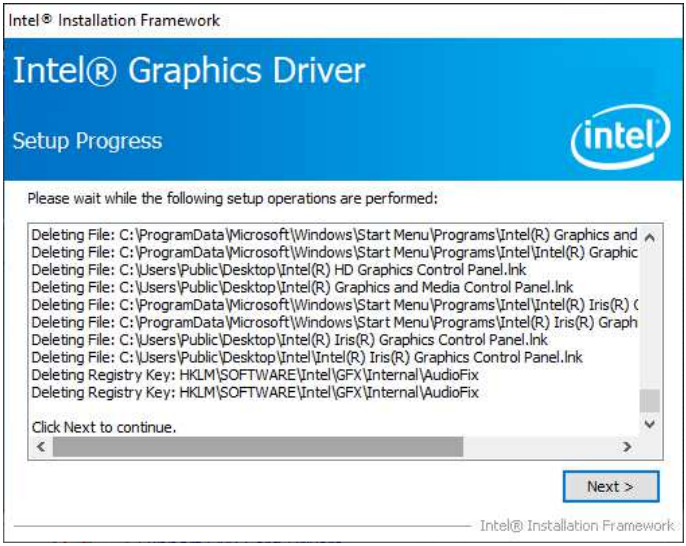

4. Click **Yes** to agree with the license agreement and continue the installation.



5. On the *Readme File Information* screen, click **Next** to continue.




6. While Setup is in progress, click **Next** to continue.




7. When installation is complete, click **Finish** to restart the computer and for changes to take effect.

## 3.4 HD Audio Driver Installation

1. Insert the disk enclosed in the package with the board. Click **Intel** and then **Intel(R) Coffeelake Chipset Drivers**.


2. Click **Realtek High Definition Audio Driver**.


3. On the *Welcome* screen of the InstallShield Wizard, click **Next** to start the installation.

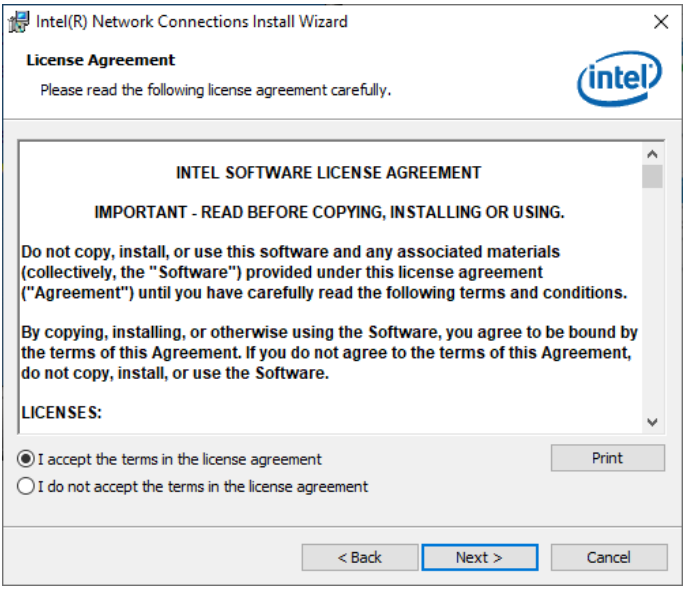
4. When installation is complete, click **Finish** to restart the computer and for changes to take effect.

## 3.5 LAN Driver Installation

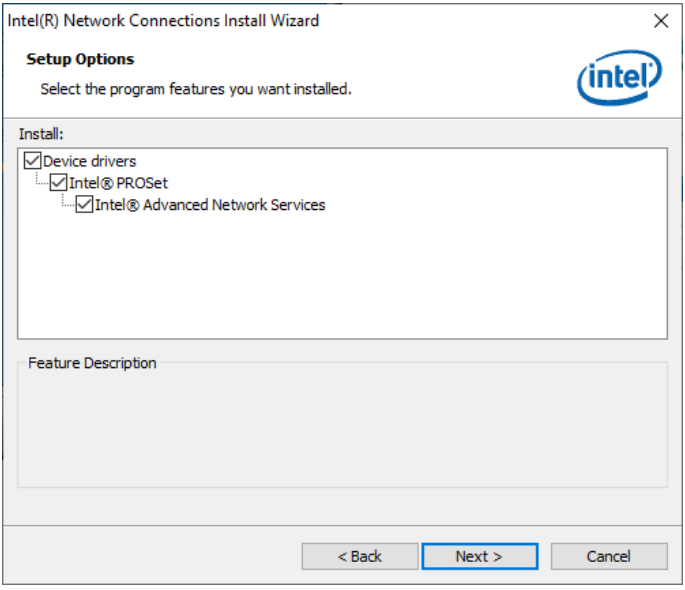
1. Insert the disk enclosed in the package with the board. Click **Intel** and then **Intel(R) Coffeelake Chipset Drivers**.


2. Click Intel(R) PRO LAN Network Drivers.

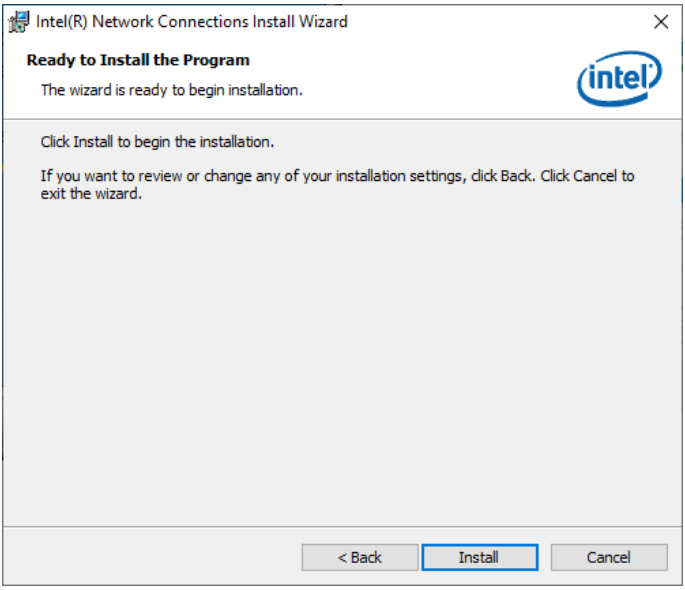
3. Click **Next** to accept the terms in the license agreement.



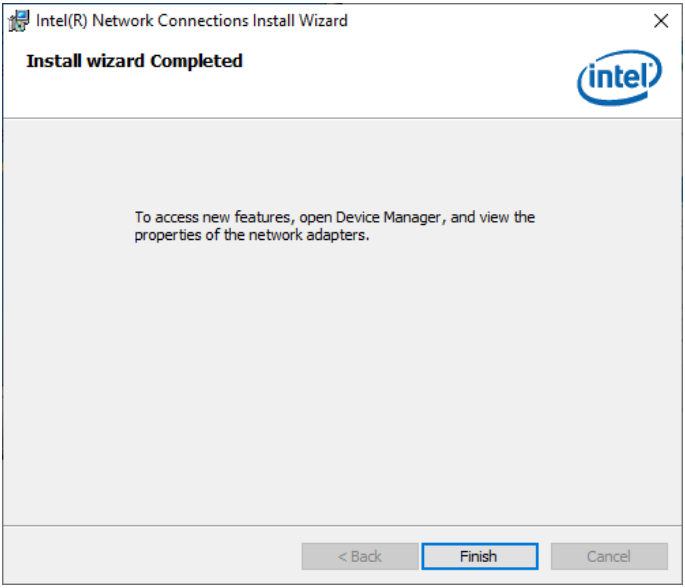

4. Click **Next** after checking the device drivers in the Setup options.



5. Click **Install** to continue.




6. When Install wizard is completed, click **Finish**.

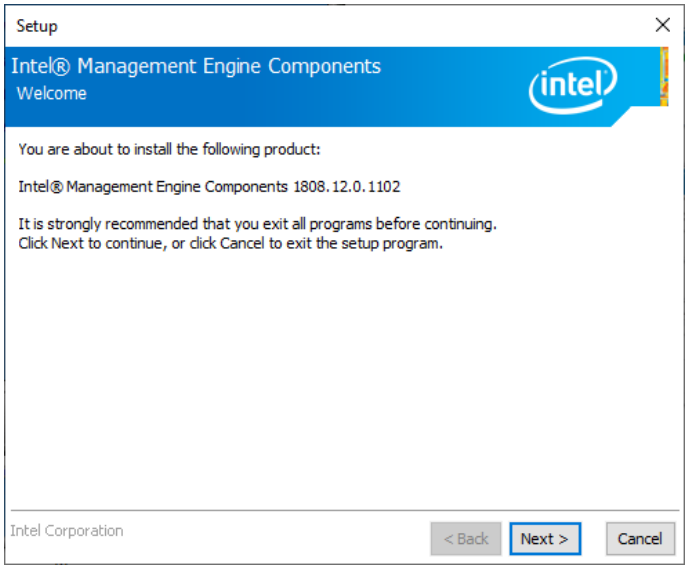


## 3.6 Intel® Management Engine Interface

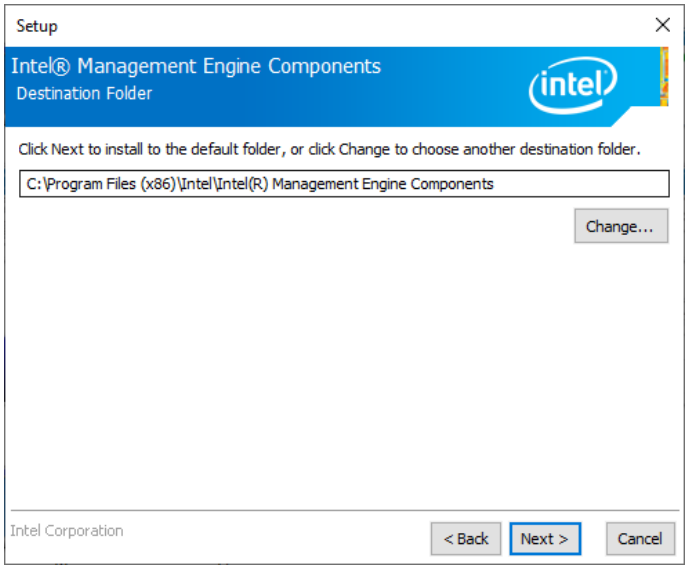
1. Insert the disk enclosed in the package with the board. Click **Intel** and then **Intel(R) Coffeelake Chipset Drivers**.


2. Click **Intel(R) ME 12.x Drivers**.

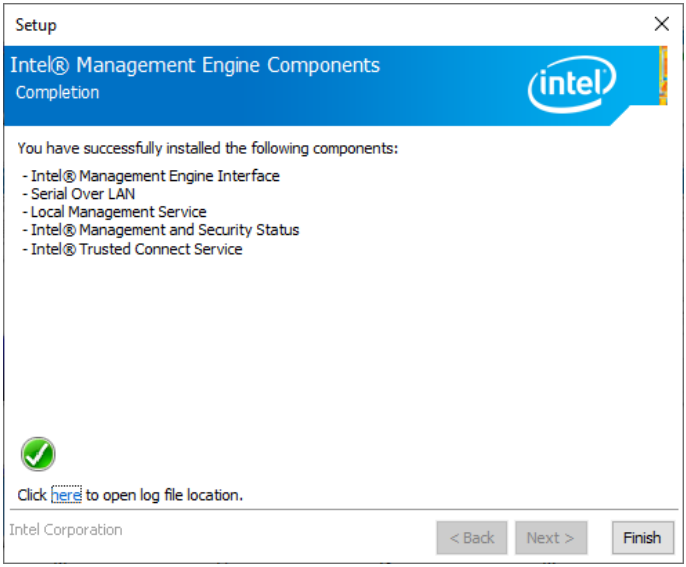
3. When the *Welcome* screen appears, click **Next**.




4. Then next window shows the destination folder where to install the files. Click **Next**.



5. After the Intel® Management Engine Components have been installed, click **Finish**.



# Chapter 4
# BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

- Main Settings
- Advanced Settings
- Chipset Settings
- Security Settings
- Book Settings
- Save & Exit

## 4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

## 4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the ”Reset” button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys.
You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press  <DEL>  to  Enter  Setup
```

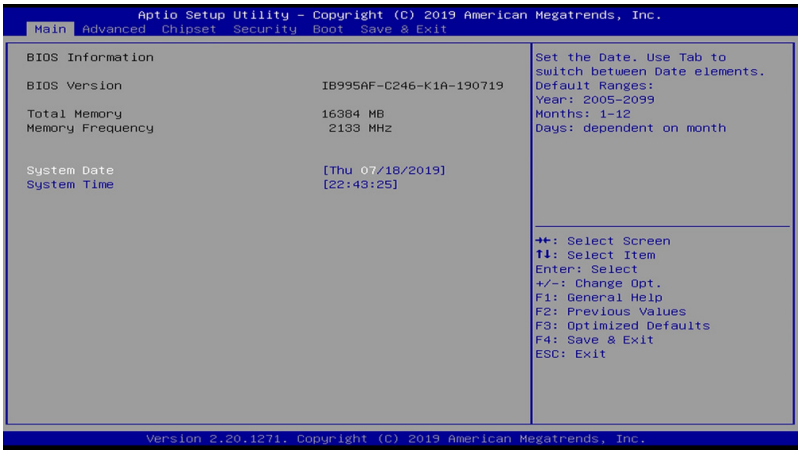
In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

**Warning:** It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

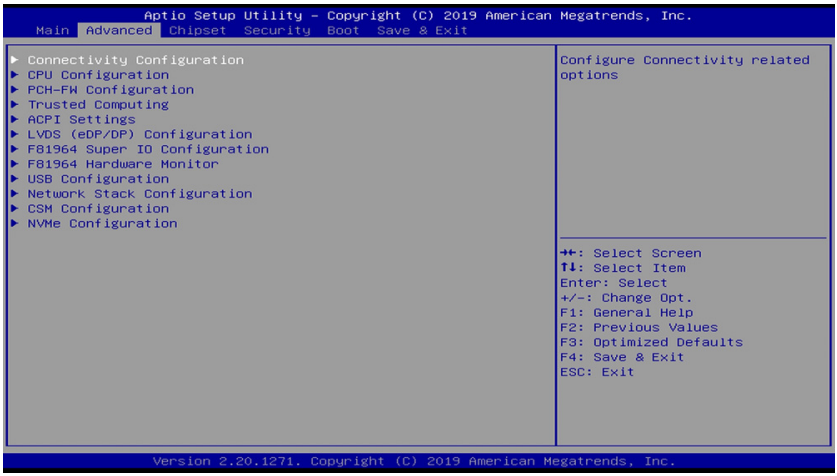
## 4.3 Main Settings



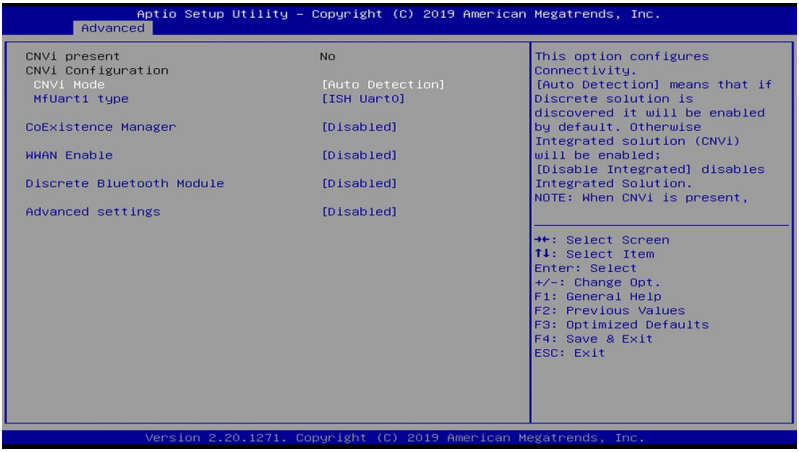

| BIOS Setting | Description |
|---|---|
| System Date | Sets the date. Use the <Tab> key to switch between the data elements. |
| System Time | Set the time. Use the <Tab> key to switch between the data elements. |

## 4.4 Advanced Settings

This section allows you to configure, improve your system and allows you to set up some system features according to your preference.

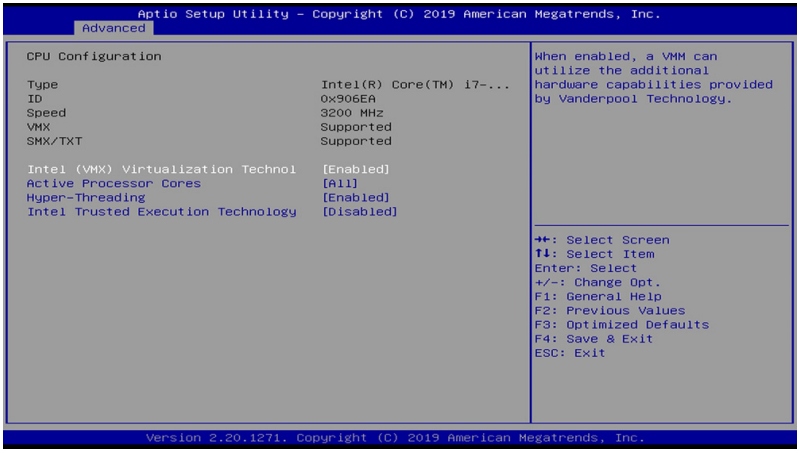


### 4.4.1 Connectivity Configuration



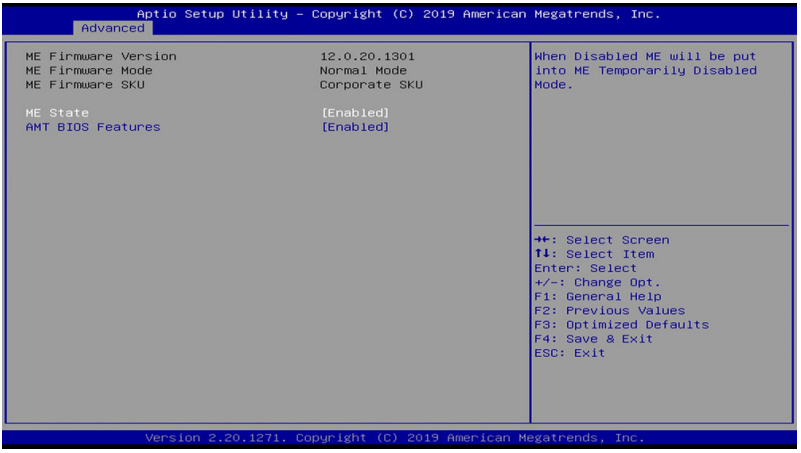

| BIOS Setting | Description |
|---|---|
| CNVi Mode | This option configures Connectivity<br>[Auto Detection] means that if Discrete solution is discovered it will be enabled by default. Otherwise Integrated solution (CNVi) will be enabled;<br>[Disable Integrated] disables integrated solution. |
| CNVi Mode | This option configures Connectivity<br>[Auto Detection] means that if Discrete solution is discovered it will be enabled by default. Otherwise integrated solution (CNVi) will be enabled; [Disable Integrated] disables integrated solution. |
| MfUart1 type | This is a test option which allows configuration of UART type for WiFi side band communication. Options are ISH Uart0, SerialIO Uart2, Uart over external pads, Not connected. |
| CoExistence Manager | CoEx Manager mitigates radio coexistence issues between Intel WWAN (modem) and Intel WLAN (WiFi/BT). This should be enabled only if both WWAN and WLAN solutions are based on Intel components. |
| WWAN Enable | Enables/Disables M.2 WWAN module. WWAN can only be enabled for re-work board. |
| Discrete Bluetooth Module | SerialIo UART0 needs to be enabled to select BT Module |
| Advanced settings | Configure ACPI objects for wireless devices |

### 4.4.2 CPU Configuration



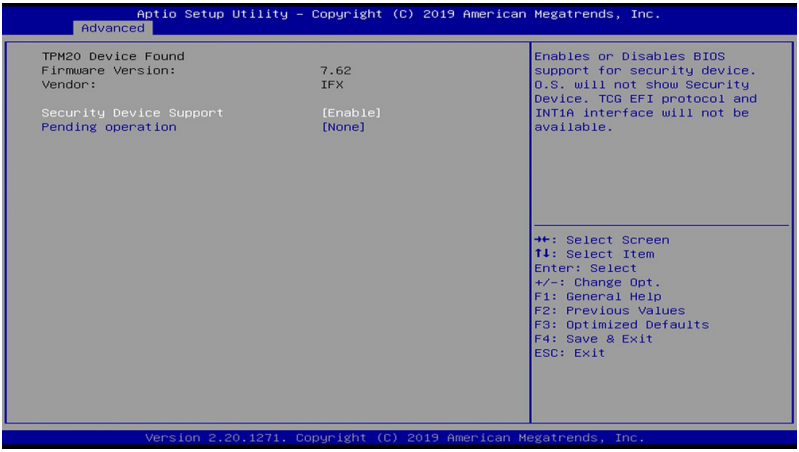

| BIOS Setting | Description |
|---|---|
| Intel (VMX) Virtualization Techno1 | When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology |
| Active Processor Cores | Number of cores to enable in each processor package. Options are All, 1, 2, 3, 4, 5 |
| Hyper-Threading | Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). |
| Intel Trusted Execution Technology | Enables utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology.<br>Changes require a full power cycle to take effect. |

### 4.4.3 PCH-FW Configuration



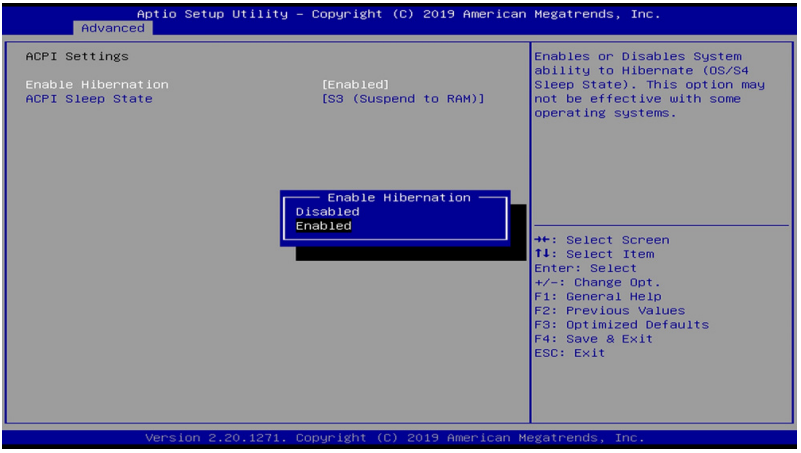

| BIOS Setting | Description |
|---|---|
| ME State | When disabled, ME will be put into ME Temporarily Disabled Mode |
| AMT BIOS Features | When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. |

### 4.4.4 Trusted Computing



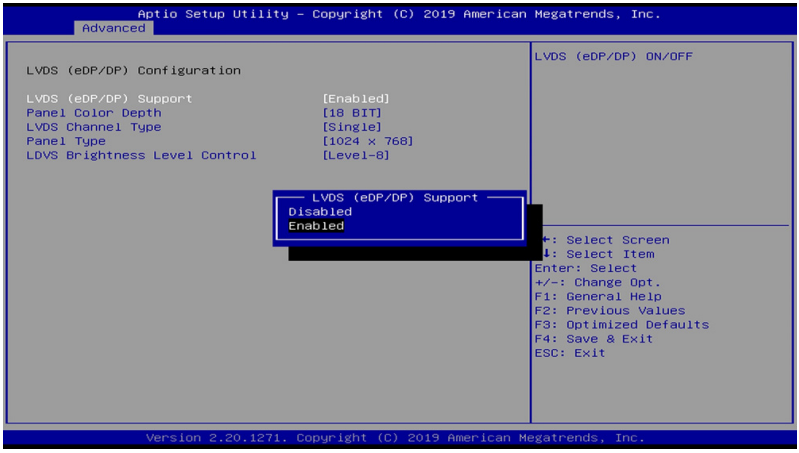

| BIOS Setting | Description |
|---|---|
| Security Device Support | Enables / Disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INTIA interface will not be available. |
| Pending Operation | Schedule an operation for the Security Device. NOTE: Your computer will reboot during restart in order to chnge State of Security Device. |

### 4.4.5 ACPI Settings



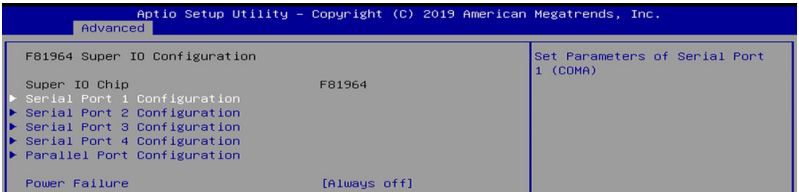

| BIOS Setting | Description |
|---|---|
| Enable Hibernation | Enables / Disables the system ability to hibernate (OS/S4 Sleep State). This option may be not be effective with some operating systems. |
| ACPI Sleep State | Selects the highest ACPI sleep state the system will enter when the suspend button is pressed.<br>Options: Suspend Disabled, S3 (Suspend to RAM) |

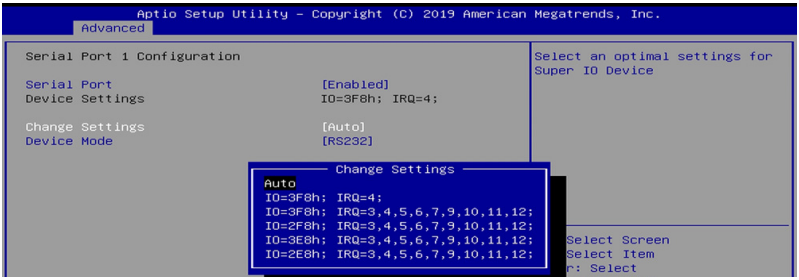
### 4.4.6 LVDS (eDP/DP) Configuration




| BIOS Setting | Description |
|---|---|
| LVDS (eDP/DP) Support | LVDS (eDP/DP) ON/OFF |
| Panel Color Depth | Options: 18 BIT, 24bit(VESA), 24bit(JEIDA) |
| LVDS Channel Type | Options: Single, Dual |
| Panel Type | Options: 800x480, 800x600, 1024x768, 1280x768, 1280x800, 1280x960, 1280x1024, 1366x768, 1440x900, 1600x900, 1600x1200, 1680x1050, 1920x1080, 1920x1200 |
| LVDS Brighntess Level Control | Options: Level-1, Level-2, Level-3, Level -4, Level-5, Level-6, Level-7, Level-8 |

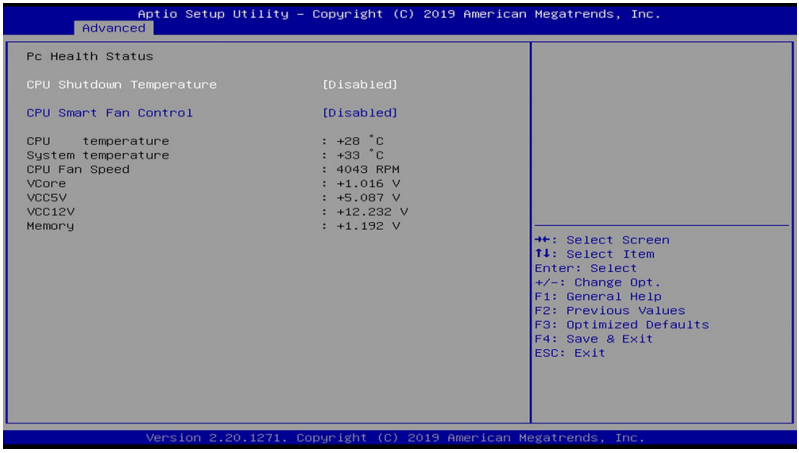
### 4.4.7 F81964 Super IO Configuration



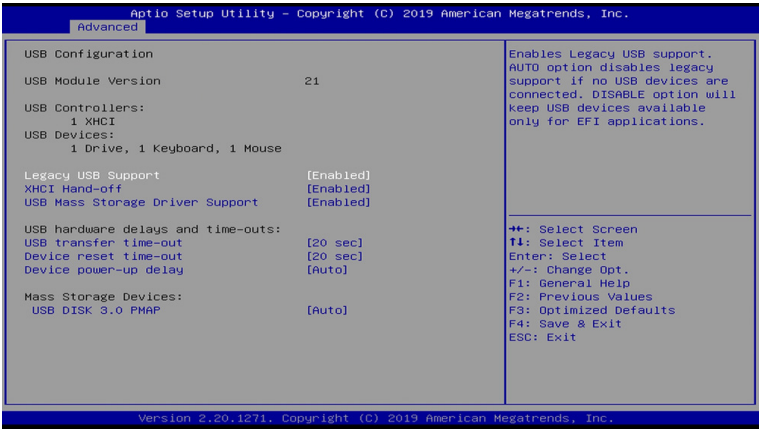

| BIOS Setting | Description |
|---|---|
| Serial Port Configuration | Sets parameters of serial ports.<br>Enables / Disables the serial port and select an optimal setting for the Super IO device. |
| Parallel Port Configuration | Set parameters of parallel port (LPT/LPTE) |
| Power Failure | Options: Always on, Always off |

### 4.4.8 F81964 Hardware Monitor



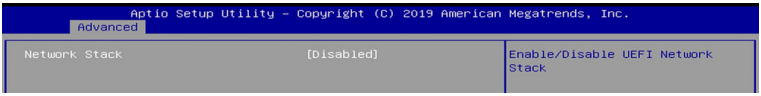

| BIOS Setting | Description |
|---|---|
| CPU Shutdown Temperature | Options: Disabled / 70 °C / 75 °C / 80 °C / 85 °C / 90 °C / 95 °C |
| CPU Smart Fan Control | Enables / Disables the CPU smart fan feature.<br>Options: Disabled / 50 °C / 60 °C / 70 °C / 80 °C |
| Temperatures / Voltages | These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status. |

### 4.4.9 USB Configuration

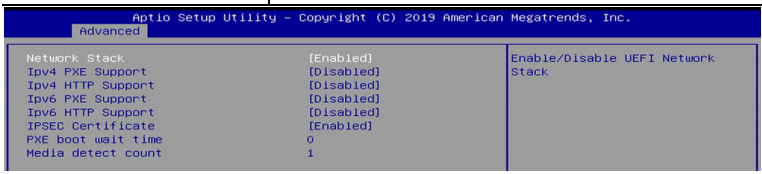



| BIOS Setting | Description |
|---|---|
| Legacy USB Support | Enables Legacy USB support.<br>“Auto” disables legacy support if there is no USB device connected.<br>“Disable” keeps USB devices available only for EFI applications. |
| XHCI Hand-off | This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver. |
| USB Mass Storage Driver Support | Enables / Disables the support for USB mass storage driver. |
| USB Transfer time-out | The time-out value for Control, Bulk, and Interrupt transfers. |
| Device reset time-out | USB mass storage device start unit command time-out. Options: 10/20/30/40 sec |
| Device power-up delay | Maximum time the device will take before it properly reports itself to the Host Controller. ‘Auto’ uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor |
| USB Disk 3.0 PMAP | Mass storage device emulation type. ‘Auto’ enumerates devices according to their media format. Optical drives are emulated as ‘CDROM’, drives with no media will be emulated according to a drive type |

### 4.4.10 Network Stack Configuration

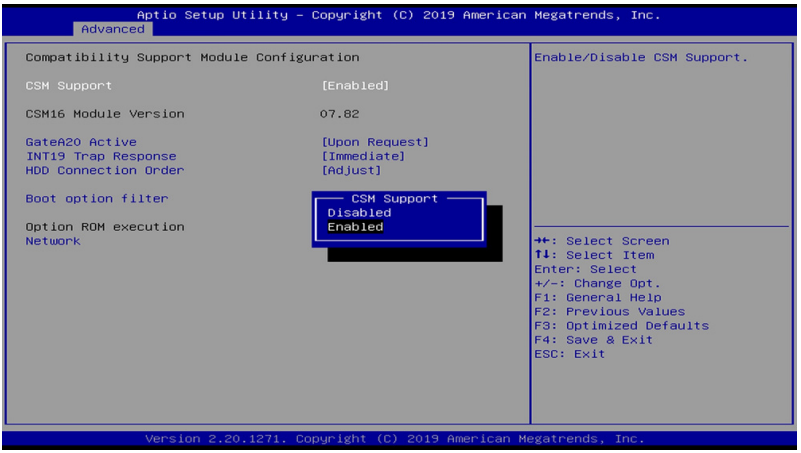



| BIOS Setting | Description |
|---|---|
| Network Stack | Enable/Disable UEFI Network Stack |




| BIOS Setting | Description |
|---|---|
| Ipv4 PXE Support | Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available |
| Ipv4 HTTP Support | Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available |
| Ipv4 PXE Support | Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available |
| Ipv6 HTTP Support | Enable/Disable IPv6 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available |
| Ipv6 PXE Support | Enable/Disable IPv6 PXE boot support. If disabled, IPv4 PXE boot support will not be available |
| IPSEC Certificate | Support to Eable/Disable IPSEC certificate for Ikey. |
| PXE boot wait time | Wait time in seconds to press ESC key to aboart the PXE boot. Use either +/1 or numeric keys to set the value |
| Media detect count | Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value |

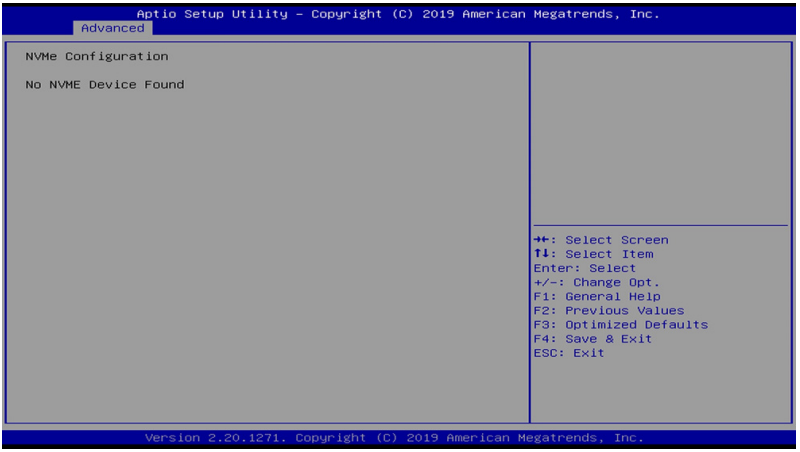
### 4.4.11 CSM Configuration



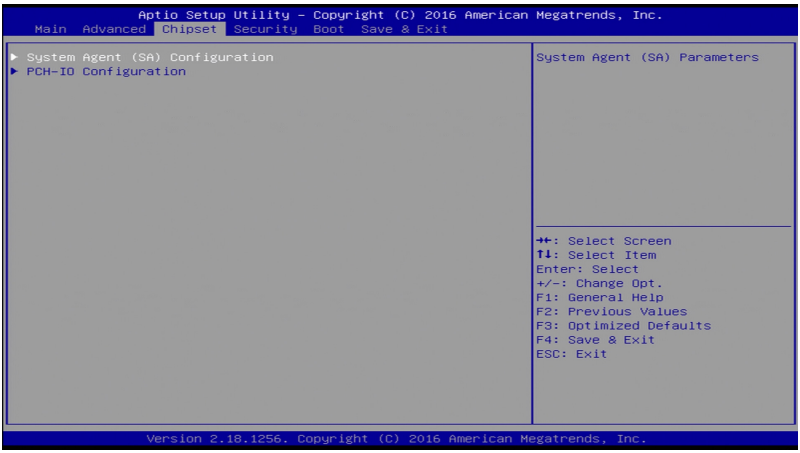

| BIOS Setting | Description |
|---|---|
| CSM Support | Enables / Disables CSM support. |
| GateA20 Active | UPON REQUEST – GA20 can be disable using BIOS services.<br>ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB. |
| INT19 Trap Response | BIOS reaction on INT19 trapping by option ROM:<br>IMMEDIATE - execute the trap right away;<br>POSTPONED – execute the trap during legacy boot. |
| HDD Connection Order | Some OS require HDD handles to be adjusted, i.e. OS is installed on drive 80h. |
| Boot option filter | This option controls Legacy/UEFI ROMs priority<br>Options: UEFI and Legacy / Legacy only / UEFI only |
| Network | Controls the execution of UEFI and Legacy PXE OpROM.<br>Options: Do not launch / Legacy |

### 4.4.12 NVMe Configuration

This sets the NVMe Device Options.

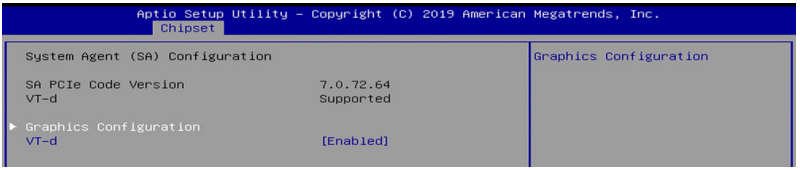


## 4.5 Chipset Settings

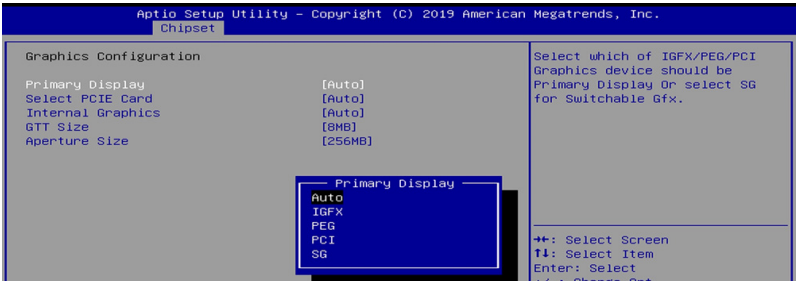



| BIOS Setting | Description |
|---|---|
| System Agent (SA) Configuration | System Agent (SA) parameters |
| PCH-IO Configuration | PCH parameters |

### 4.5.1 System Agent (SA) Configuration

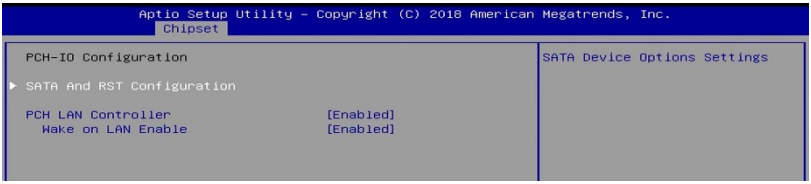



#### 4.5.1.1 Graphics Configuration and VT-d Capability

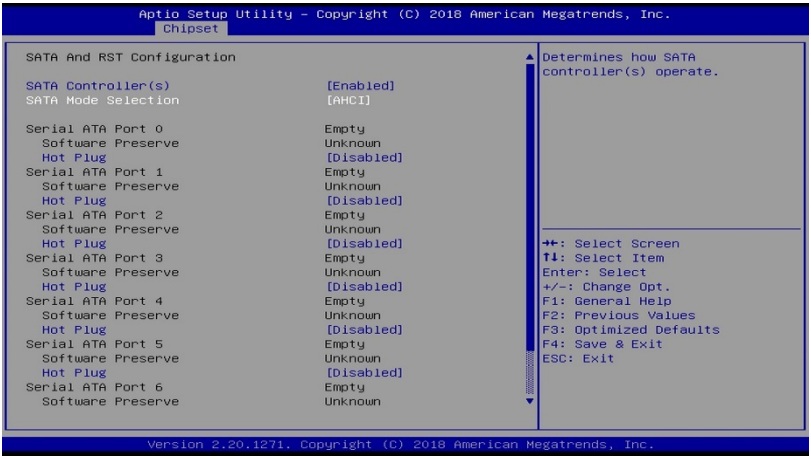



| BIOS Setting | Description |
|---|---|
| Primary Display | Selects which of IGFX/PEG/PCI graphics device should be primary display, or selects SG for switchable Gfx. |
| Select PCIE Card | Select the card used on the platform.<br>Auto: Skip GPIO basd Power Enable to dGPU<br>Elk Creek 4: DGPU Power Enable =ActiveLow<br>PEG Eval: DGPU Power Enable = ActiveHigh |
| Internal Graphics | Keeps IGFX enabled based on the setup options. |
| GTT Size | Select the GTT Size<br>Options: 2MB / 4MB / 8MB |
| Aperture Size | Select the Aperture Size<br>Note: Above 4MB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.<br>Options: 128MB / 256MB / 512MB / 1024MB / 2048MB |

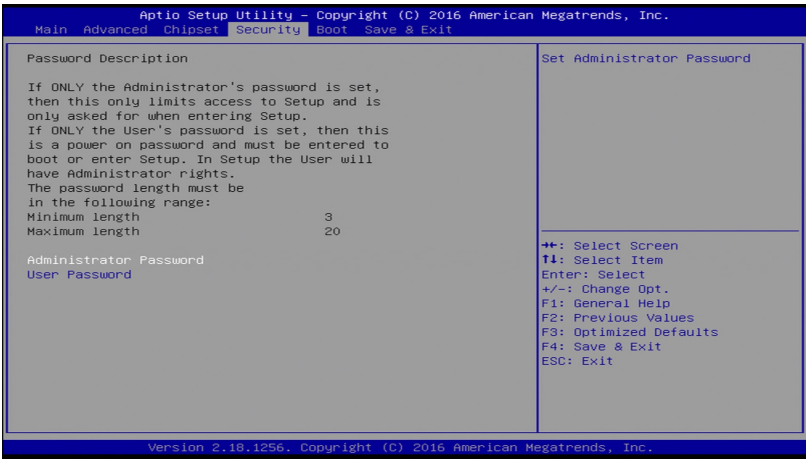
### 4.5.2 PCH-IO Configuration




| BIOS Setting | Description |
|---|---|
| SATA and RST Configuration | Configures SATA devices. |
| PCH LAN Controller | Enables / Disables the onboard NIC. |
| Wake on LAN Enable | Enables / Disables the integrated LAN to wake up the system. |

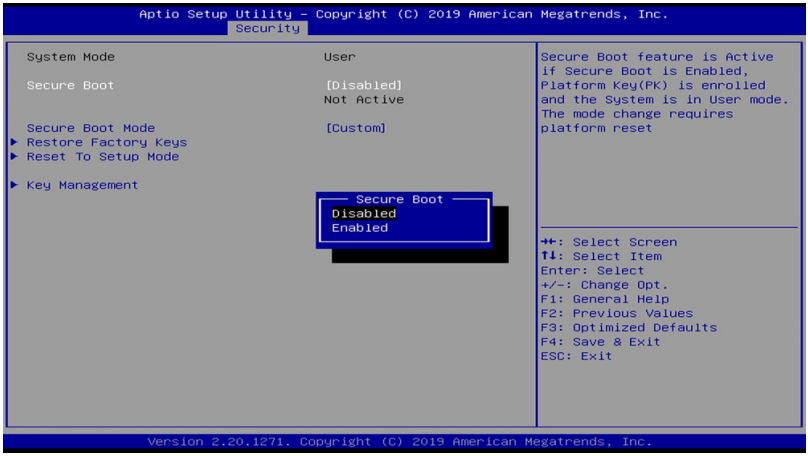


## 4.6 Security Settings



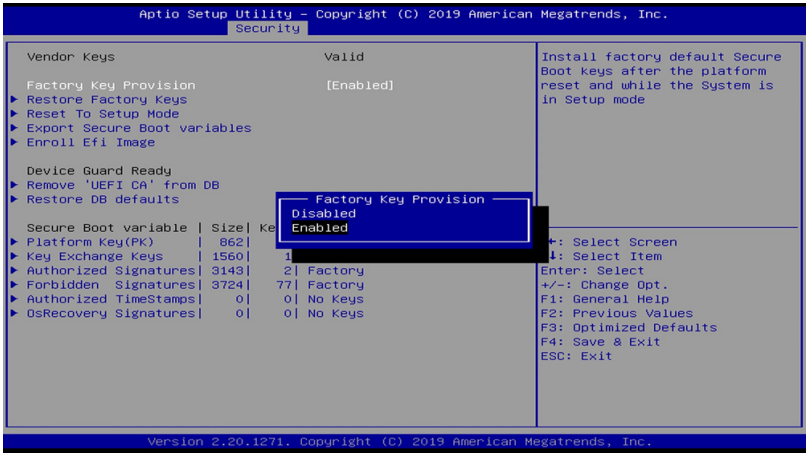

| BIOS Setting | Description |
|---|---|
| Administrator Password | Sets an administrator password for the setup utility. |
| User Password | Sets a user password. |

### 4.6.1 Secure Boot Configuration

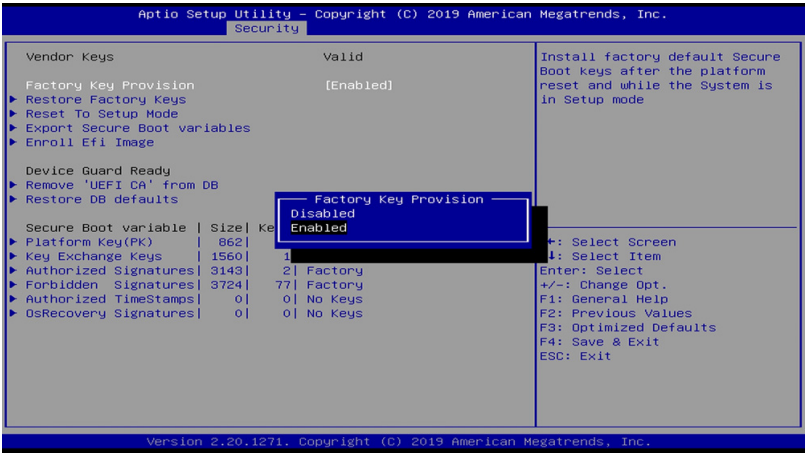



| BIOS Setting | Description |
|---|---|
| Secure Boot | Secure Boot feature is active if Secure Boot enabled. Platform Key(PK) is enrolled and the system is in user mode. The mode change requires platform reset. |
| Secure Boot Mode | Secure Boot mode options:<br>Standard or Custom.<br>In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication. |
| Restore Factory Keys | Force System to User Mode. Install factory default Secure Boot key databases. |
| Reset To Setup Mode | Delete all Secure Boot key databases from NVRAM |
| Key Management | Enables expert users to modify Secure Boot Policy variables without full authentication |

### 4.6.1.1 Key Management

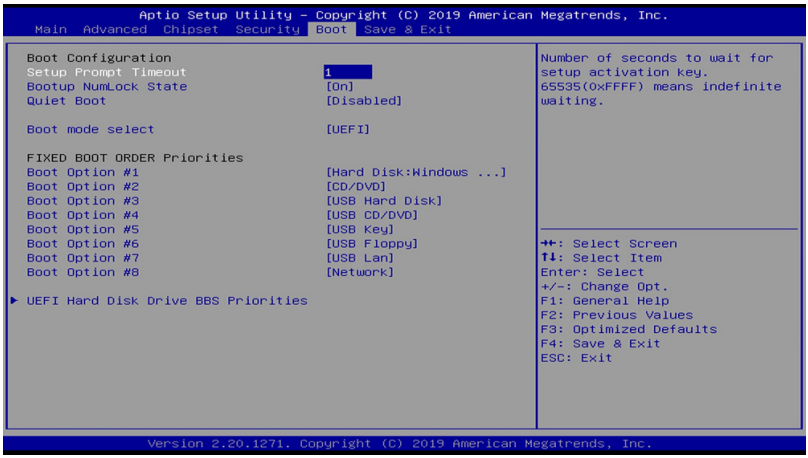



| BIOS Setting | Description |
|---|---|
| Factory Key Provision | Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode. |
| Restore Factory Keys | Force System to User Mode. Install factory default Secure Boot key databases. |
| Reset To Setup Mode | Delete all Secure Boot key databases from NVRAM |
| Export Secure Boot variables | Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device |
| Enroll Efi Image | Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database(db) |
| Remove ‘UEFI CA’ from DB | Device Guard ready system must not list ‘Microsoft UEFI CA’ Certificate in Authorized Signature database (db) |
| Restore DB defaults | Restore DB defaults to factory defaults |



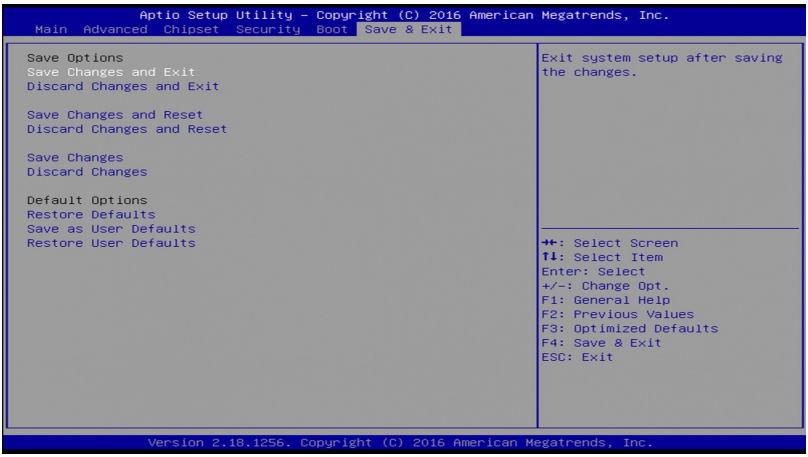

| | |
|---|---|
| Secure Boot variable<br><br>Platform Key(PK)<br>Key Exchange Keys<br>Authorized Signatures<br>Forbidden Signatures<br>Authorized TimeStamps<br>OsRecovery Signatures | Enroll Factory Defaults or load certificates from a file:<br>1. Public Key Certificate:<br>a) EFI_SIGNATURE_LIST<br>b) EFI_CERT_X509 (DER)<br>c) EFI_CERT_RSA2048 (bin)<br>d) EFI_CERT_SHAXXX<br>2. Authenticated UEFI Variable<br>3. EFI PE/COFF Image(SHA256)<br>Key Source:<br>Factory, External, Mixed |

## 4.7 Boot Settings




| BIOS Setting | Description |
|---|---|
| Setup Prompt Timeout | Number of seconds to wait for setup activation key.<br>65535(0xFFFF) means indefinite waiting. |
| Bootup NumLock State | Selects the keyboard NumLock state. |
| Quiet Boot | Enables / Disables Quiet Boot option. |
| Boot mode select | Select boot mode LEGACY/UEFI |
| FIXED BOOT ORDER Priorities | Sets the system boot order. |
| UEFI Hardk Disk Drive BBS Priorities | Specifies the Boot Device Priority UEFI Hard Disk Drives |

## 4.8 Save & Exit Settings




| BIOS Setting | Description |
|---|---|
| Save Changes and Exit | Exits system setup after saving the changes. |
| Discard Changes and Exit | Exits system setup without saving any changes. |
| Save Changes and Reset | Resets the system after saving the changes. |
| Discard Changes and Reset | Resets system setup without saving any changes. |
| Save Changes | Saves changes done so far to any of the setup options. |
| Discard Changes | Discards changes done so far to any of the setup options. |
| Restore Defaults | Restores / Loads defaults values for all the setup options. |
| Save as User Defaults | Saves the changes done so far as User Defaults. |
| Restore User Defaults | Restores the user defaults to all the setup options. |

# Appendix

This section provides the mapping addresses of peripheral devices and the sample code of watchdog timer configuration.

# A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

| Address | Device Description |
|---|---|
| 0000h-0CF7h | PCI Express Root Complex |
| 0040h-0043h | System timer |
| 0050h-0053h | System timer |
| 0070h-0070h | System CMOS/real time clock |
| 00F0h-00F0h | Numeric data processor |
| 02E8h-02EFh | Communications Port (COM4) |
| 02F8h-02FFh | Communications Port (COM2) |
| 03B0h-03BBh | Intel(R) HD Graphics 530 |
| 03C0h-03DFh | Intel(R) HD Graphics 530 |
| 03E8h-03EFh | Communications Port (COM3) |
| 03F8h-03FFh | Communications Port (COM1) |
| 0D00h-FFFFh | PCI Express Root Complex |
| E000h-0E01h | Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #6 - A115 |
| F000h-F03Fh | Intel(R) HD Graphics 530 |
| F040h-F05Fh | Intel(R) 100 Series/C230 Series Chipset SMBus - A123 |
| F060h-F07Fh | Standard SATA AHCI Controller |
| F080h-F083h | Standard SATA AHCI Controller |
| F090h-F097h | Standard SATA AHCI Controller |
| F0A0h-F0A7h | Intel(R) Active Management Technology - SOL (COM5) |

# B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

| Level | Function |
|---|---|
| IRQ0 | System Timer |
| IRQ3 | Serial Port #2 |
| IRQ4 | Serial Port #1 |
| IRQ5 | Serial Port #3 |
| IRQ7 | Serial Port #4 |
| IRQ8 | Real Time Clock |
| IRQ 11 | Intel(R) 100 Series/C230 Series Chipset Family Integrated Sensor Hub - A135 |
| IRQ 11 | Intel(R) 100 Series/C230 Series Chipset SMBus - A123 |
| IRQ 11 | Intel(R) 100 Series/C230 Series Chipset Thermal subsystem - A131 |
| IRQ 13 | Numeric data processor |
| IRQ 16 | High Definition Audio Controller |
| IRQ 16 | Standard SATA AHCI Controller |
| IRQ 19 | Intel(R) Active Management Technology - SOL (COM5) |

# C. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

### Sample Code:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv());
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv())
{
                unsigned char bBuf;
                unsigned char bTime;
                char **endptr;

                char SIO;

                printf("Fintek 81866 watch dog program\n");

                SIO = Init_F81866();
                if (SIO == 0)
                {
                                printf("Can not detect Fintek 81866, program abort.\n");
                                return(1);
                }//if (SIO == 0)

                if (argc != 2)
                {
                                printf(" Parameter incorrect!!\n");
                                return (1);
                }

                bTime = strtol (argv(1), endptr, 10);
                printf("System will reset after %d seconds\n", bTime);

                if (bTime)
                {               EnableWDT(bTime);           }
                else
```

```
		{		DisableWDT();		}

		return 0;
}
//---------------------------------------------------------------------------
void EnableWDT(int interval)
{
		unsigned char bBuf;

		bBuf = Get_F81866_Reg(0x2B);
		bBuf &= (~0x20);
		Set_F81866_Reg(0x2B, bBuf);		//Enable WDTO

		Set_F81866_LD(0x07);
		//switch to logic device 7
		Set_F81866_Reg(0x30, 0x01);		//enable timer

		bBuf = Get_F81866_Reg(0xF5);
		bBuf &= (~0x0F);
		bBuf |= 0x52;
		Set_F81866_Reg(0xF5, bBuf);		//count mode is second

		Set_F81866_Reg(0xF6, interval);		//set timer

		bBuf = Get_F81866_Reg(0xFA);
		bBuf |= 0x01;
		Set_F81866_Reg(0xFA, bBuf);		//enable WDTO output

		bBuf = Get_F81866_Reg(0xF5);
		bBuf |= 0x20;
		Set_F81866_Reg(0xF5, bBuf);		//start counting
}
//---------------------------------------------------------------------------
void DisableWDT(void)
{
		unsigned char bBuf;

		Set_F81866_LD(0x07);
		//switch to logic device 7

		bBuf = Get_F81866_Reg(0xFA);
		bBuf &= ~0x01;
		Set_F81866_Reg(0xFA, bBuf);
		//disable WDTO output

		bBuf = Get_F81866_Reg(0xF5);
		bBuf &= ~0x20;
		bBuf |= 0x40;
		Set_F81866_Reg(0xF5, bBuf);
		//disable WDT
}
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
```

```
//---------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
	unsigned int result;
	unsigned char ucDid;

	F81866_BASE = 0x4E;
	result = F81866_BASE;

	ucDid = Get_F81866_Reg(0x20);
	if (ucDid == 0x07)
	//Fintek 81866
	{	goto Init_Finish;	}

	F81866_BASE = 0x2E;
	result = F81866_BASE;

	ucDid = Get_F81866_Reg(0x20);
	if (ucDid == 0x07)
	//Fintek 81866
	{	goto Init_Finish;	}

	F81866_BASE = 0x00;
	result = F81866_BASE;

Init_Finish:
	return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81866 (void)
{
	outportb(F81866_INDEX_PORT, F81866_UNLOCK);
	outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81866 (void)
{
	outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, F81866_REG_LD);
	outportb(F81866_DATA_PORT, LD);
	Lock_F81866();
}
//---------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, REG);
	outportb(F81866_DATA_PORT, DATA);
	Lock_F81866();
}
//---------------------------------------------------------------------------
unsigned char Get_F81866_Reg(unsigned char REG)
{
	unsigned char Result;
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, REG);
	Result = inportb(F81866_DATA_PORT);
	Lock_F81866();
	return Result;
}
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
```

```
//---------------------------------------------------------------------------
#ifndef __F81866_H
#define __F81866_H                                          1
//---------------------------------------------------------------------------
#define         F81866_INDEX_PORT                   (F81866_BASE)
#define         F81866_DATA_PORT                    (F81866_BASE+1)
//---------------------------------------------------------------------------
#define         F81866_REG_LD                       0x07
//---------------------------------------------------------------------------
#define F81866_UNLOCK                               0x87
#define         F81866_LOCK                                 0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif          //__F81866_H
```