06 High-speed input counter

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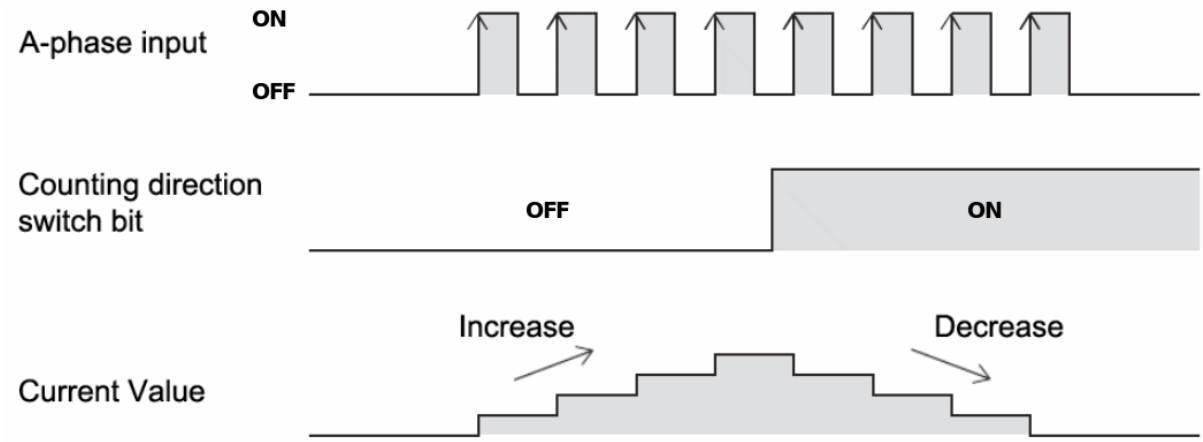
Specifications of high-speed counter

Types of high-speed counters

(1) Single-phase input counter (S/W)

The counting method of single-phase input counter (S/W) is as follows:

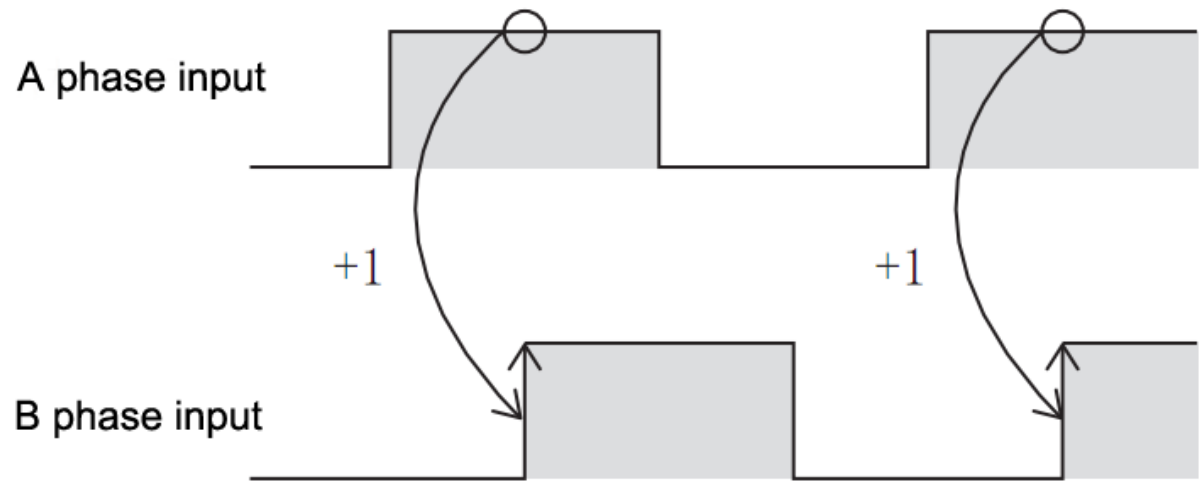


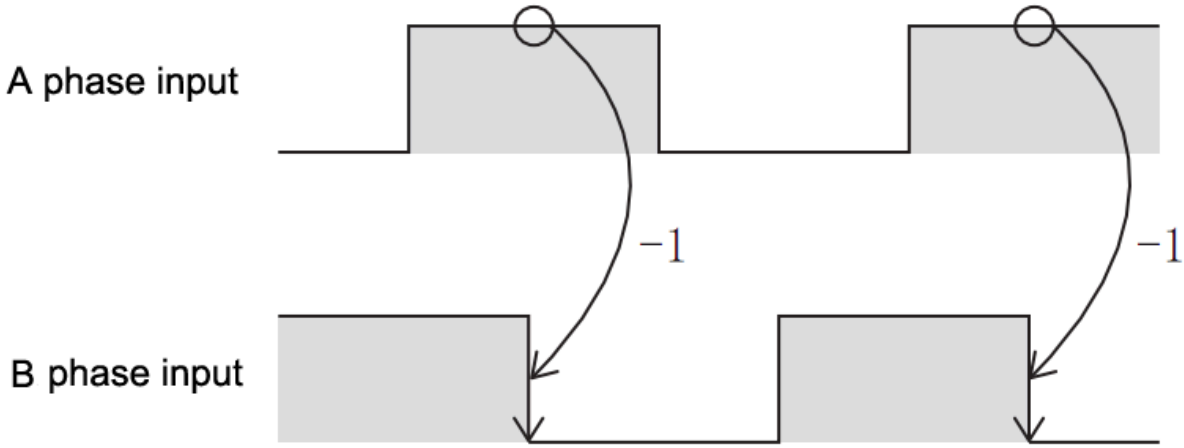
(2) AB phase input counter [1 times frequency]

The counting method of AB phase input counter [1 times frequency] is as follows:

Increase/decrease action	Timing
When counting up	Phase A input is ON and phase B input is OFF→ON, the count will increase by 1
When counting down	When the A phase input is ON and the B phase input is ON→OFF, the count will decrease by 1

When counting up When counting down



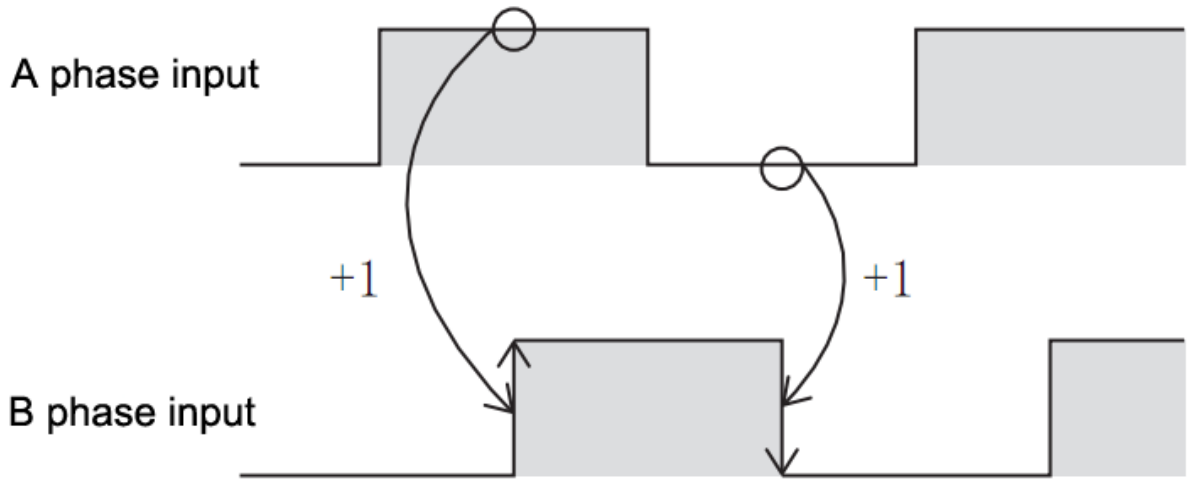


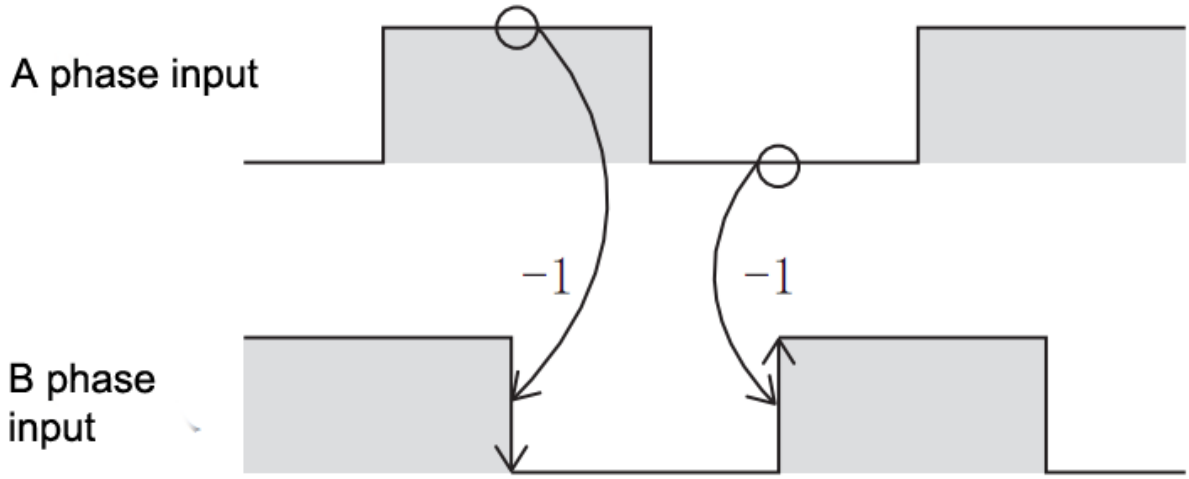
(3) AB phase input counter [2 times frequency]

The counting method of 2-phase 2-input counter [2 times frequency] is as follows:

Increase/decrease action	Timing
When counting up	When the A phase input is ON and the B phase input is OFF→ON, the count will increase by 1; The count will increase by 1 when the phase A input is OFF and the phase B input is ON→OFF.
When counting down	When A phase input is ON and B phase input is ON→OFF, the count will decrease by 1; When phase A input is OFF and phase B input changes from OFF→ON, the count will decrement by 1.

When counting up When counting down



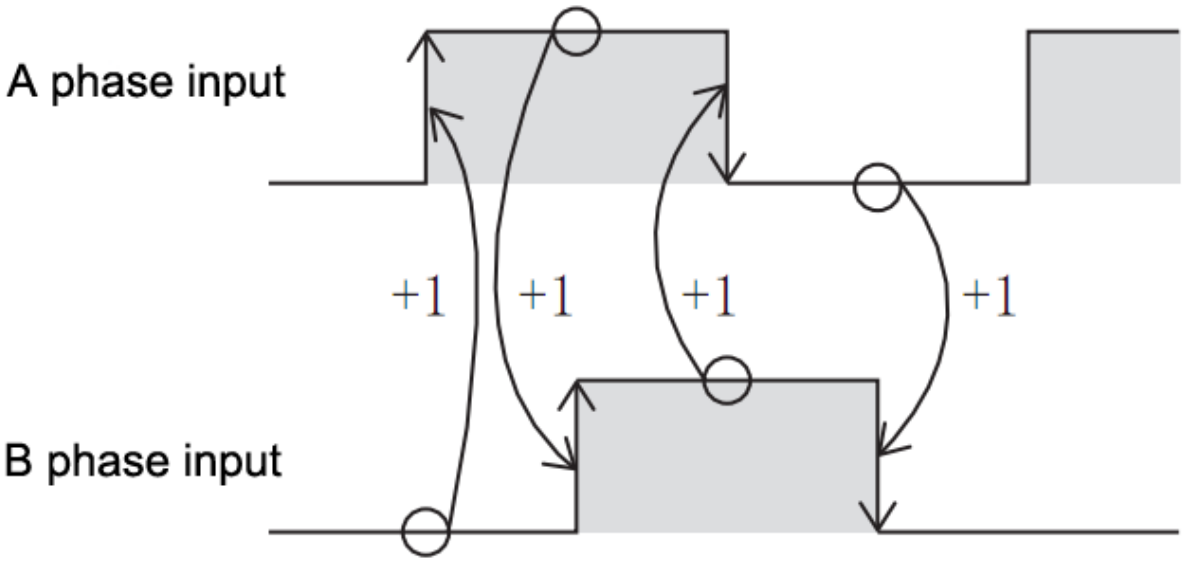


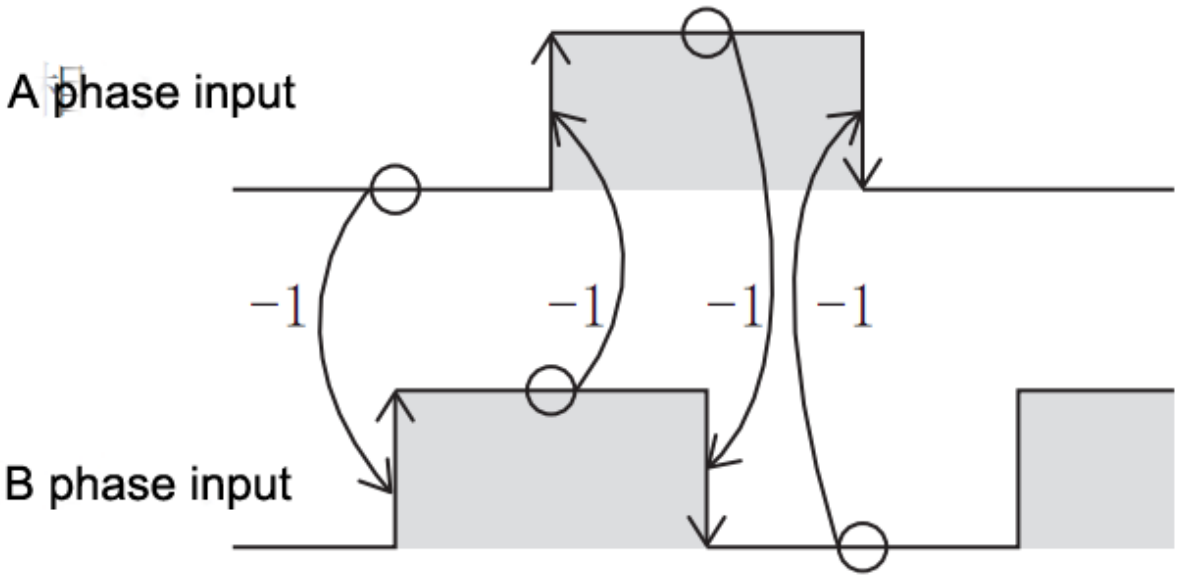
(4) AB phase input counter [4 times frequency]

The counting method of 2-phase 2-input counter [4 times frequency] is as follows:

Increase/decrease action	Timing
When counting up	When B phase input is OFF and A phase input is OFF→ON, the count will increase by 1; When the A phase input is ON and the B phase input is OFF→ON, the count will increase by 1; When B phase input is ON and A phase input is ON→OFF, the count will increase by 1; The count will increase by 1 when the phase A input is OFF and the phase B input is ON→OFF.
When counting down	When A phase input is OFF and B phase input is OFF→ON, the count will decrease by 1; When B phase input is ON and A phase input is OFF→ON, the count will decrease by 1; When A phase input is ON and B phase input is ON→OFF, the count will decrease by 1; When Phase B input is OFF and Phase A input is ON→OFF, the count will decrement by 1.

When counting up When counting down





Highest frequency

The maximum countable frequency of various high-speed counters is as follows:

Counter type	Highest frequency
Single phase input counter (S/W)	150KHz
AB phase input counter [1 times frequency]	100KHz
AB phase input counter [2 times frequency]	100KHz
AB phase input counter [4 times frequency]	100KHz

Counting range: -2147483648 to 2147483647, which is a signed 32-bit ring counter.

High-speed counter allocation

The input soft components of various types of high-speed counters are fixedly allocated, including 8 channels HSC0 to HSC7.

Each channel can be changed to single-phase input or AB-phase input according to the high-speed counter configuration, but it should be noted that the occupied X point cannot be repeated.

Channel	High-speed counter type	X0	X1	X2	X3	X4	X5	X6	X7	X10	X11	X12	X13	X14	X15	X16	X17
HSC0	Single phase input (S/W)	A															
	AB phase input	A	B														
HSC1	Single phase input (S/W)		A														
	AB phase input			A	B												
HSC2	Single phase input (S/W)			A													
	AB phase input					A	B										
HSC3	Single phase input (S/W)				A												
	AB phase input							A	B								
HSC4	Single phase input (S/W)					A											
	AB phase input									A	B						
HSC5	Single phase input (S/W)						A										
	AB phase input											A	B				
HSC6	Single phase input (S/W)							A									
	AB phase input													A	B		
HSC7	Single phase input (S/W)								A								

AB phase input — A B

A: Phase A input B: Phase B input

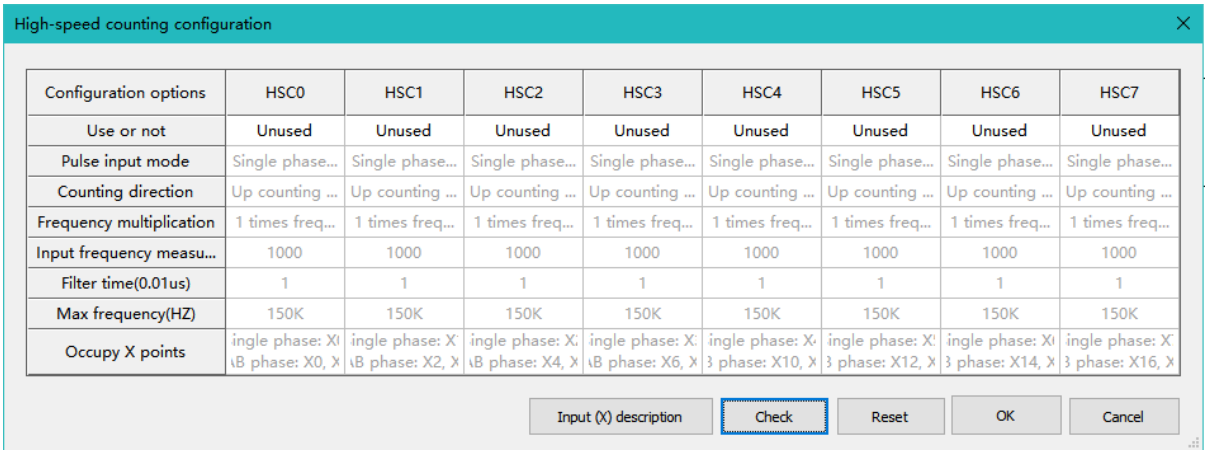
#Note: After HSC0 uses the AB phase input, HSC1 can no longer use single-phase input, because HSC0 occupies two points X0 and X1, and if HSC1 wants to use single-phase input, X1 needs to be occupied and conflicts occur. The same is true for other channels.

High-speed counter use steps

The following describes the steps to use the high-speed counter.

"Project management" → "Parameter" → "High-speed counter configuration"

(1) Screen display



(2) Display content

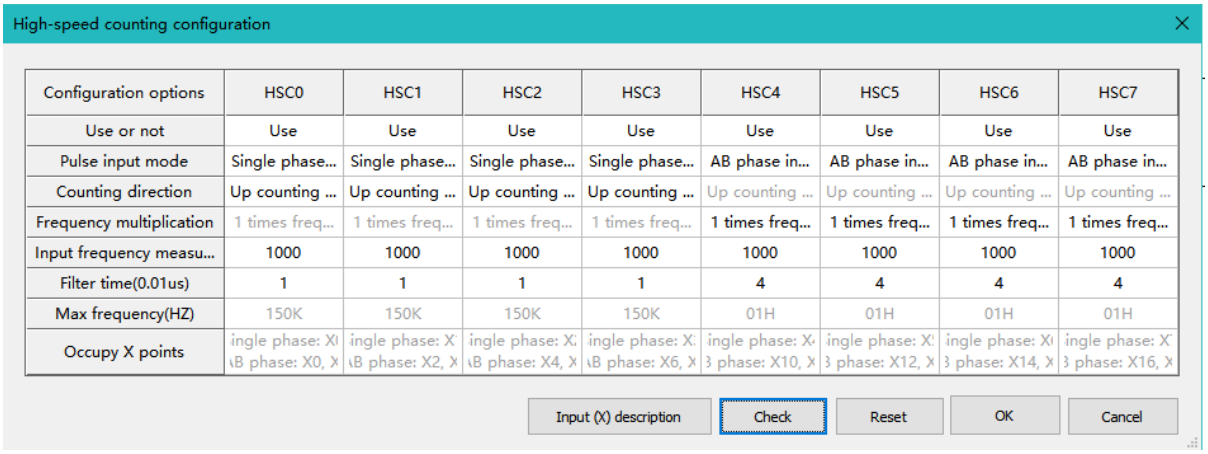
Parameter	Range	Instruction
Use or not	Use/not use	Set whether to use the counter.
Pulse input	Single phase input	Choose to use single phase input or AB pha
mode	AB phase input	
Counting direction	Up counting mode down counting mode	Select up/down counting mode, valid only w
Frequency multiplication	One times frequency	Select input count multiplier, only valid whe
	two times frequency	
	four times frequency	
Input frequency test time (ms)	1 to 32767(ms)	Set how often the input frequency is measu measurement result is output in the special register.
Filter time	0 to 1700(0.01us)	Set the X point of this channel as the filter ti but the anti-interference ability will be reduc
		When the input is 0, it is the lowest filter t
Highest frequency	Single phase input: 150K	Display the highest input frequency that eac
	AB phase input: 100K	
Occupy X points	-	Show which X points are occupied after usi
Check button		Check whether the configured X input point input
Restore to default		Restore to the same default settings as abo

Input (X) description　　Pop up the description table of all modes of

Confirm input　　After the configuration is complete, click to

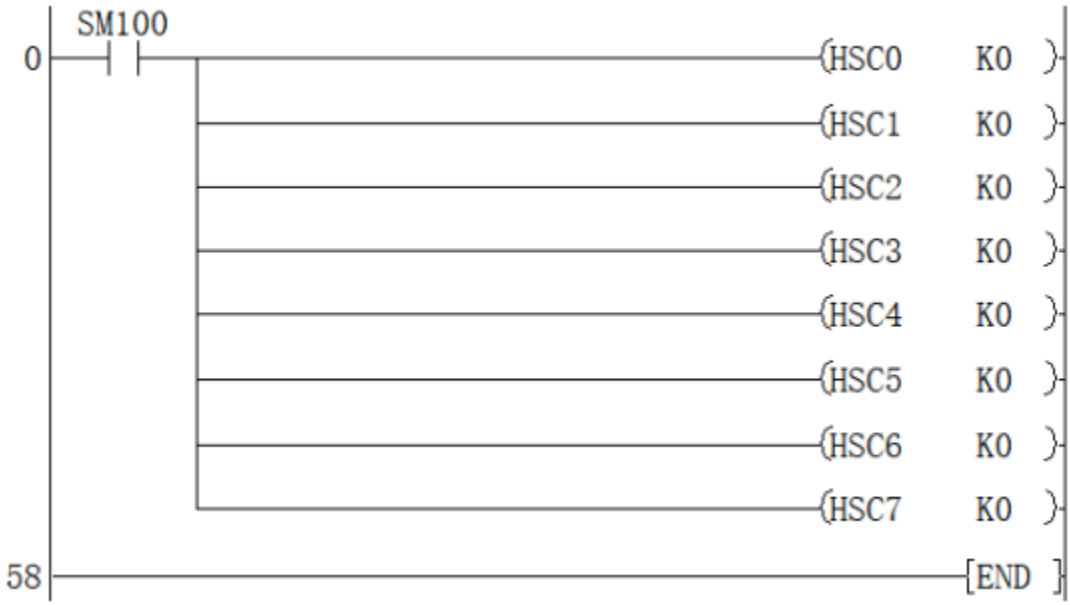
(3) Configuration example

HSC0 to HSC3 are configured as 4 single-phase inputs, and HSC4 to HSC7 are configured as 4 AB phase inputs.



Configuration options	HSC0	HSC1	HSC2	HSC3	HSC4	HSC5	HSC6	HSC7
Use or not	Use	Use	Use	Use	Use	Use	Use	Use
Pulse input mode	Single phase...	Single phase...	Single phase...	Single phase...	AB phase in...	AB phase in...	AB phase in...	AB phase in...
Counting direction	Up counting ...	Up counting ...	Up counting ...	Up counting ...	Up counting ...	Up counting ...	Up counting ...	Up counting ...
Frequency multiplication	1 times freq...	1 times freq...	1 times freq...	1 times freq...	1 times freq...	1 times freq...	1 times freq...	1 times freq...
Input frequency measu...	1000	1000	1000	1000	1000	1000	1000	1000
Filter time(0.01us)	1	1	1	1	4	4	4	4
Max frequency(HZ)	150K	150K	150K	150K	01H	01H	01H	01H
Occupy X points	ingle phase: X(\B phase: X0, X	ingle phase: X' \B phase: X2, X	ingle phase: X; \B phase: X4, X	ingle phase: X: \B phase: X6, X	ingle phase: X- 3 phase: X10, X	ingle phase: X' 3 phase: X12, X	ingle phase: X(3 phase: X14, X	ingle phase: X' 3 phase: X16, X

Use the OUT HSC instruction in the main program to enable High-speed counter. At this time, as long as there is an external pulse input, the pulse value can be observed in HSC0 to HSC7.



In the double word composed of special soft components SD403 and SD402, the current input pulse frequency of HSC0 can be monitored. Other channels also have corresponding registers, please refer to the description of special registers for details.

If the counter need to be stopped, just turn off the OUT HSC instruction.

High-speed counter instructions

OUT HSC/High-speed counter switch

When the operation result before the OUT HSC instruction is ON, the high-speed counter is turned on. At this time, the value of the HSC register records the number of high-speed pulses currently received. If the count value is reached, the corresponding HSC bit register becomes on.

-[OUT (d) (value)]

Content, range and data type

Parameter	Content	Range	Data type	Data type (label)
(d)	High-speed counter channel	HSC0 to HSC7	Signed BIN 32 bit	ANY32
(value)	High-speed counter setting value	-2147483648 to 2147483647	Signed BIN 32 bit	ANY32

Device used

Instruction	Parameter	Devices									Offset modification	Pulse extension
		KnX	KnY	KnM	KnS	D	R	SD	HSC	K	[D]	XXP
OUT HSC	Parameter 1								●			
	Parameter 2	●	●	●	●	●	●	●		●		

Features

To enable or disable high-speed counter counting, please configure the high-speed input channel to use the high-speed counter. For details, refer to the high-speed counter description.

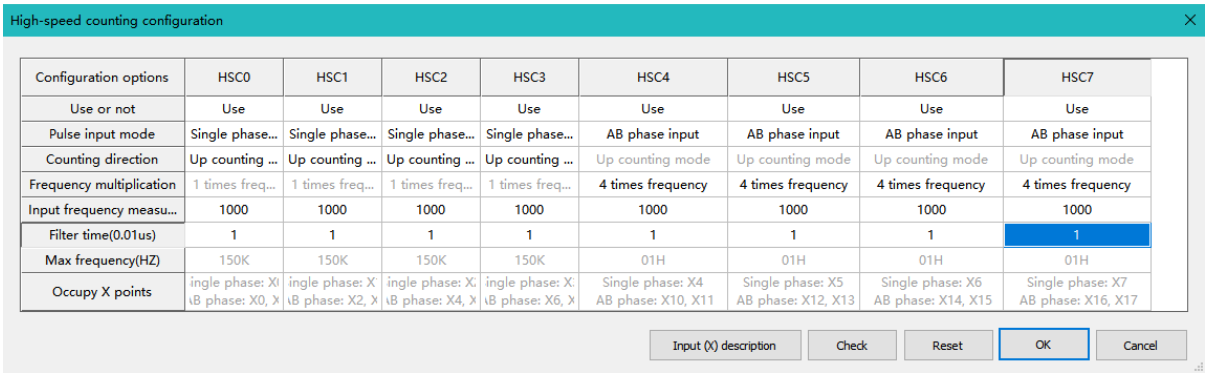
Operation result before instruction	Action	HSC data register status	HSC bit register status
ON	Turn on High-speed counter	The value is accumulated according to the input pulse	Turn ON when the value reaches the set value, otherwise OFF
OFF	Stop High-speed counter	The value remains the same	State remains unchanged

Error code

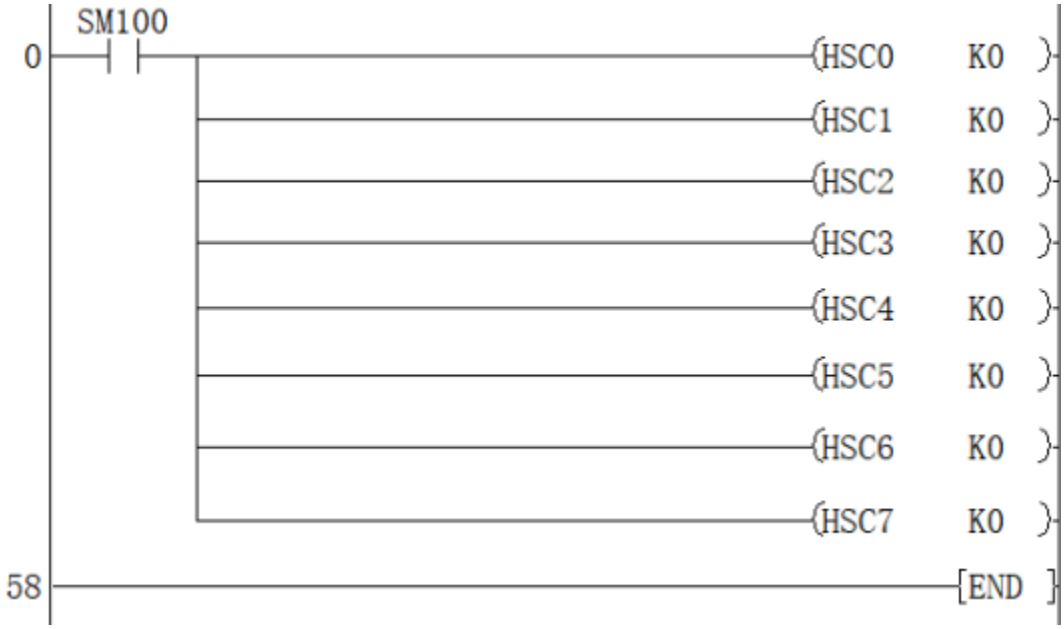
Error code	Content
4085H	(value) The read address exceeds the device range
2580H	After the high-speed counter is turned on, but the axis high-speed counter enable is not configured

Example

HSC0 to HSC3 are configured as 4 single-phase inputs, and HSC4 to HSC7 are configured as 4 AB phase inputs.

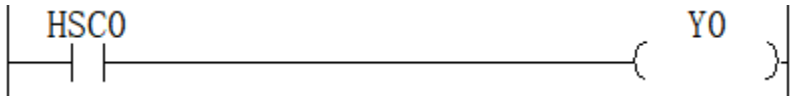


Use the OUT HSC instruction in the main program to enable High-speed counter. At this time, as long as there is an external pulse input, the pulse value can be observed in HSC0 to HSC7.



In the double word composed of special soft components SD403 and SD402, the current input pulse frequency of HSC0 can be monitored. Other channels also have corresponding registers, please refer to the description of special registers for details.

When the value of HSC0 is greater than 0, the contact of HSC0 will be set, and the other channels are the same. As shown in the circuit program below, Y0 will be turned on.



DHSCS/High-speed comparison set

Comparing the counted value in the high-speed counter with the specified value each time it counts, and then immediately set the bit device instruction.

-[DHSCS (s1) (s2) (d)]

Content, range and data type

Parameter

(s1) data compared with the current value of the high-speed counter, or the word device number where the data to be compared is stored

(s2) high-speed counter device

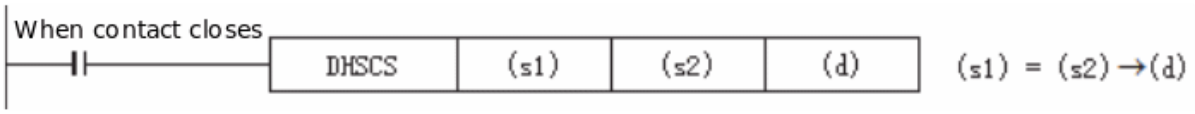
(d) device number set (ON) when they match

Device used

Instruction	Parameter	Devices														Offset modification		Pulse extension
		Y	M	S	SM	D.b	KnX	KnY	KnM	KnS	T	C	R	SD	LC	HSC	H	[D]	XXP
DHSCS	Parameter 1						●	●	●	●	●	●	●	●	●	●	●		
	Parameter 2															●			
	Parameter 3	●	●	●	●	●													

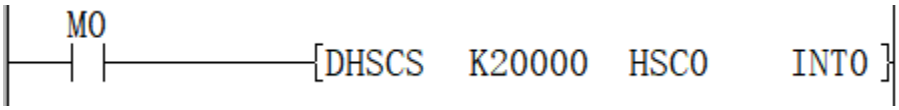
Features

• When the current value of the high-speed counter of the channel specified in (s2) becomes the comparison value (s1) (in the case of the comparison value K200, 199→200 and 201→200), regardless of the scan time, the bit device (d) Both will be set (ON). This instruction performs comparison processing after the counting processing of the high-speed counter.



• If the device specified in (d) is Y0 to Y20, when (d) is set, Y will be directly mapped to the actual hardware output, regardless of the scan cycle.

• DHSCS parameter 3 can also use the interrupt function name as a parameter. As shown in the figure below, the interrupt program INT0 will be executed when HSC0 is from (19999→20000) or (20001→20000).



#Note:

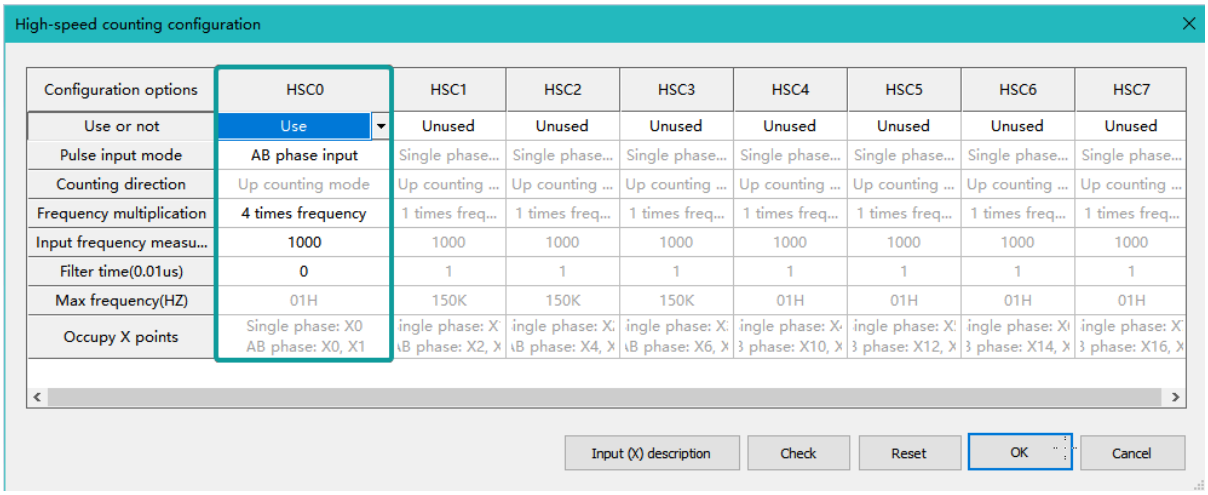
The high-speed counter interrupt only supports a total of 100 programs, and each DHSCS is also counted in these 100. If it exceeds, an operation error will be reported.

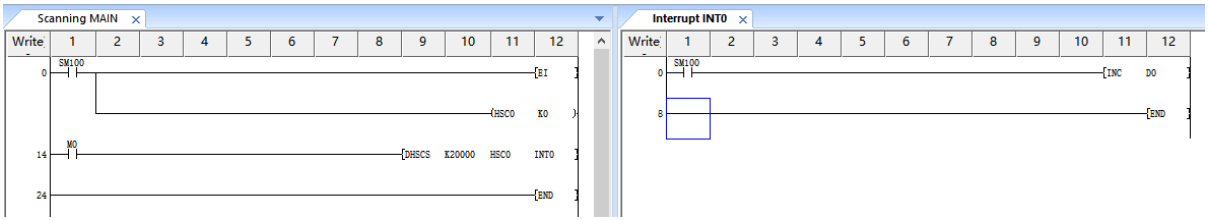
Error code

Error code	Content
4084H	The input device in (s2) exceeds the range of HSC0 to HSC7
4085H	(s1) and (s2) read addresses exceed the device range
4086H	(d) write address exceeds the device range
2406H	The number of high-speed counter interrupts exceeds 100
4F81H	DHSCS,SHSCR and DHSZ runs,but OUT HSC does not program

Example

To configure the high-speed counter, take HSC0 as an example.





In scanning MAIN, use the EI instruction to enable the interrupt, and then use the OUT HSC instruction to turn on the high-speed counter.

After M0 is turned on, when the value of HSC0 changes from 19999→20000, the INT0 program is executed once, that is, D0 is increased by 1.

When the value of HSC0 changes from 20000→20001, the INT0 program is not executed, that is, D0 remains at 1.

When the value of HSC0 changes from 20001→20000, the INT0 program is executed once, that is, D0 is increased by 1, and D0 is 2.

DHSCR/High-speed comparison reset

Each time it counts, compare the counted value in the high-speed counter with the specified value, and then immediately reset the bit device instruction.

-[DHSCR (s1) (s2) (d)]

Content, range and data type

Parameter

(S1) data compared with the current value of the high-speed counter, or the word device number where the data to be compared is stored

(S2) high-speed counter device

(d) device number reset (OFF) when they match

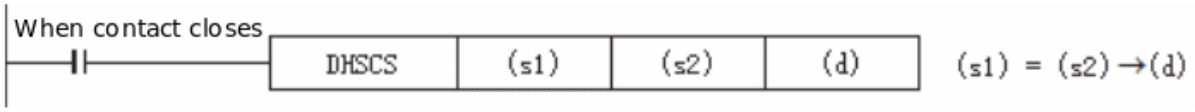
Device used

Instruction	Parameter	Devices															Offset modification		Pulse extension
		Y	M	S	SM	D	LC	KnX	KnY	KnM	KnS	T	R	SD	LC	HSC	Z	H	[D]		XXP
DHSCR	S1					●	●	●	●	●	●	●	●	●	●	●	●	●			

Parameter 2	●
Parameter 3	● ● ● ● ●

Features

• When the current value of the high-speed counter of the channel specified in (s2) becomes the comparison value (s1) (in the case of the comparison value K200, 199→200 and 201→200), regardless of the scan time, the bit device (d) Both will be reset (OFF). This instruction performs comparison processing after the counting processing of the high-speed counter.



• If the device specified in (d) is Y0 to Y20, when (d) is set, Y will be directly mapped to the actual hardware output, regardless of the scan cycle.

#Note:

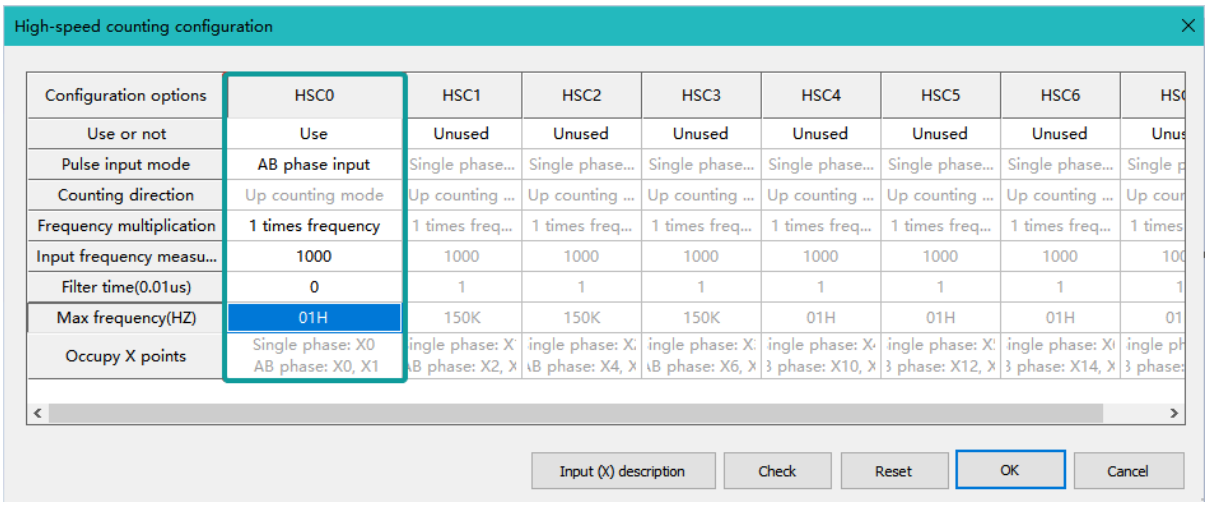
The high-speed counter interrupt only supports a total of 100 programs, and each DHSCR is also counted in these 100. If it exceeds, an operation error will be reported.

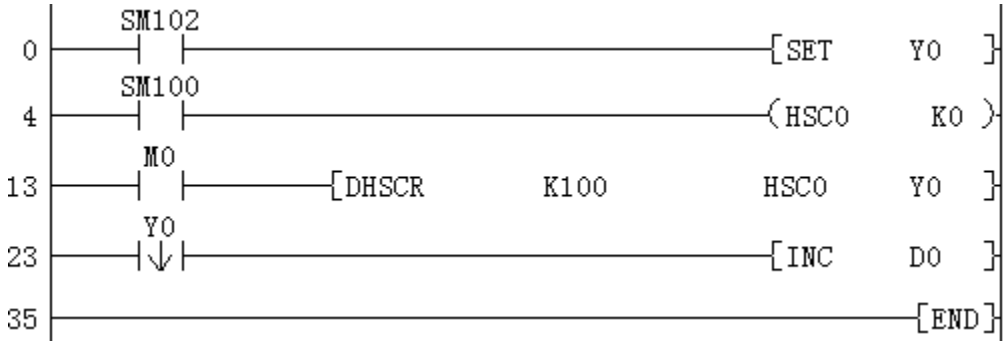
Error code

Error code	Content
4084H	The input device in (s2) exceeds the range of HSC0 to HSC7
4085H	The (s1) and (s2) read addresses exceed the device range
4086H	The (d) write address exceeds the device range
2406H	The number of high-speed counter interrupts exceeds 100
4F81H	DHSCS,SHSCR and DHSZ runs,but OUT HSC does not program.

Example

To configure the high-speed counter, use HSC0 as an example.





Use the OUT HSC instruction to turn on the high-speed counter while scanning MAIN.

After M0 is turned on, when the value of HSC0 changes from 99→100, reset Y0 and D0 will increase by 1.

DHSZ/High-speed zone comparison

The current value of the high-speed counter is compared with two values (bandwidth), and the comparison result is output.

-[DHSZ (s1) (s2) (s3) (d)]

Content, range and data type

Parameter	Content
(S1)	Data compared with the current value of the high-speed counter, or the word device number (comparison value 1) where the data to be compared is stored
(S2)	Data compared with the current value of the high-speed counter, or the word device number (comparison value 2) where the data to be compared is stored
(S3)	High-speed counter device
(d)	The device number of the start bit of the comparison result output in comparison value 1 and comparison value 2

Device used

Instruction	Parameter	Devices								
		Y	M	S	SM	D.b	KnX	KnY	KnM	K
DHSCZ	Parameter 1						●	●	●	●
	Parameter 2						●	●	●	●
	Parameter 3									
	Parameter 4	●	●	●	●	●				

Features

• Compare the current value of the high-speed counter specified in (s3) with two comparison values (comparison value 1, comparison value 2), regardless of the scan time, (d), (d)+1, (d)+2 One item in will turn ON according to the comparison result (lower, in area, upper).

• If the device specified in (d) is Y0 to Y15, when (d), (d+1), (d+2) are set, Y will be directly mapped to the actual hardware output, not affected by the scan cycle .

• When setting [Comparison Value 1] and [Comparison Value 2], please ensure that [Comparison Value 1]<[Comparison Value 2]. If the settings are different, an operation error will occur, and the DHSZ instruction will not execute the action.

#Note:

The high-speed counter interrupt only supports a total of 100 programs, and each DHSZ is also counted in these 100, and the DHSZ instruction will occupy the space of 2 interrupt programs. If it exceeds, an operation error will be reported.

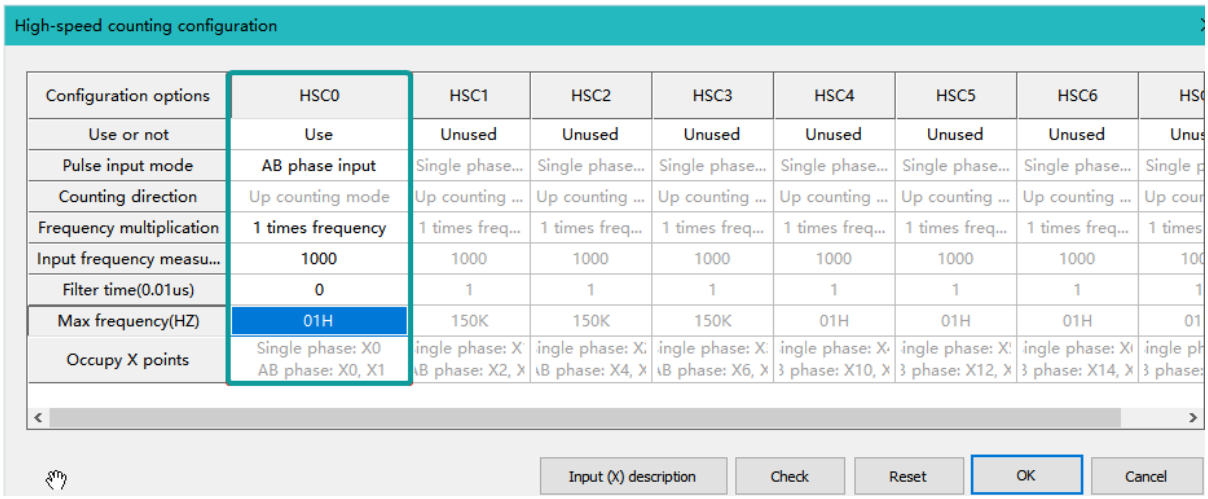
The comparison result occupies the unit of 3 consecutive addresses starting with (d). Please be careful not to overlap with other controlled devices. In addition, when specifying the Y device, please set it not to exceed the actual number of Y point outputs.

Error code

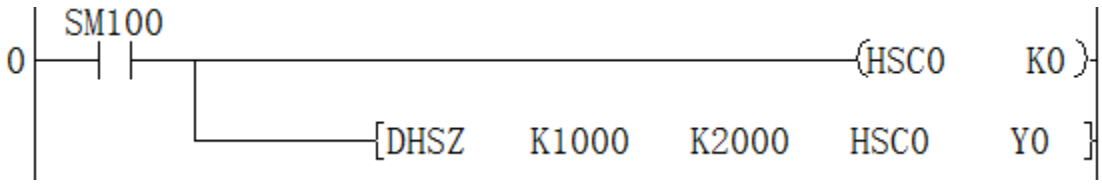
Error code	Content
4084H	(s2) The input device exceeds the range of HSC0 to HSC7
4085H	(s1)(s2) The read address exceeds the device range
4086H	(d) The write address exceeds the device range
2406H	The number of high-speed counter interrupts exceeds 100
4F81H	DHSCS,SHSCR and DHSZ runs,but OUT HSC does not program

Example

To configure the high-speed counter, use HSC0 as an example.



Scanner



Execution results

Comparison mode	**Current value of channel 1 (s3)**
(S1)>(s3)	1000>(s3)
	999→1000
	1000→999
(S1)≤(s3)≤(s2)	999→1000
	1000→999
	1000≤(s3)≤2000
	2000→2001
	2001→2000
(S3)>(s2)	2000→2001
	2001→2000
	(S3)>2000